Fault-Induced Delayed Voltage Recovery Assessment based on Dynamic Voltage Indices

Jaime D. Pinzón
Institute of Electrical Energy
National University of San Juan - CONICET
San Juan, Argentina
jpinzon@iee.unsj.edu.ar

D. Graciela Colomé
Institute of Electrical Energy
National University of San Juan - CONICET
San Juan, Argentina
colome@iee.unsj.edu.ar

***Abstract*— This paper presents a new methodology for assessing fault-induced delayed voltage recovery (FIDVR) problems in power systems based on the calculation of dynamic voltage indices. The indices allow obtaining information on the power system post-contingency dynamic behavior. As part of the methodology, the calculation of instantaneous indices (voltage index -VI), indices per time window (dynamic voltage index - DVI), per bus (DVI_b) and of the whole system (wide-area dynamic voltage index - WADVI) is proposed. These indices are compared with thresholds to determine buses with delayed voltage recovery problems. Case studies were simulated in the New England 39-bus test system in which the proposed methodology was implemented. The methodology is used to identify voltage recovery problems from a low computational time procedure, with which indices are obtained that allow determining the location and magnitude of delayed voltage recovery events.**

***Index terms*— dynamic voltage indices, FIDVR, faults, power systems.**

I. INTRODUCTION

The delayed voltage recovery, also known as fault-induced delayed voltage recovery (FIDVR), is the phenomenon by which the voltage after a fault clearance in transmission, sub-transmission or distribution systems remains low during a period of time defined by the network operator [1], [2].

Currently, FIDVR events are cause for concern because they show a temporary loss of voltage control in an area, and they pose a cascading event risk over a larger area. Especially if another unexpected event happens, while the voltage is low or a severe event that may cause a fast voltage collapse [3].

The delayed voltage recovery is a condition that produces the increase of system stress. An improper operation of the power equipment, leads to protective relays misoperation and when the control systems do not work properly the component output is produced. Moreover, when the voltages remain low for a long time, the protection systems disconnect generators or the over-excitation limiters reduce the reactive power supplied with the final system collapse [4], [5].

The FIDVR events are initiated by the stall condition of low inertia induction motors during a fault. The load characteristics such as the dynamic behavior under faults and the protection system operation increase the risk of delayed voltage recovery events [3].

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In recent years, the implementation of measurement units with higher sampling rates, such as phasor measurement units (PMU), made possible to observe that FIDVR events are more frequent than previously thought. These devices record up to 60 samples per second compared to a typical SCADA system, which scans every two - four (2-4) seconds and stores a sample in a database every one - five (1-5) minutes [3], [6]. The highest sampling rate was the key for improving the FIDVR event identification and post-event analysis [1], [3].

The post-event analysis has been vital not only find the deficiencies in the modeling of components, but also to implement the corresponding improvements and assess dynamic problems (location and magnitude) [1], [3], [4]. Traditionally, static simulations with power flow calculations have been used to assess the system's proximity to long-term voltage stability limits under several operating conditions [6]. Voltage-dependent static load models have worked well for this. However, the inability to adequately model dynamic loads has contributed to network vulnerability due to FIDVR events. Therefore, a FIDVR analysis requires time-domain dynamic simulations using dynamic models with aggregate loads that appropriately represent the penetration of induction motors [7].

In order to analyze voltage recovery problems, voltage deviation indices have been proposed in [8], voltage recovery indices in [9], an index to identify the most efficient location of load shedding to improve the voltage recovery in [10]. On the other hand, international entities of rules and regulations, such as the North American Electric Reliability Corporation (NERC), Western Electricity Coordinating Council (WECC), IEC and IEEE, settled limit values in voltage dips that lead to a delayed voltage recovery [11]. Under these bases, there is currently no methodology to assess FIDVR problems in power systems, which allows obtaining information as regards the magnitude and location of the problem.

This paper presents a new methodology for assessing FIDVR events through the calculation of instantaneous voltage indices (VI), indices per time window (DVI), per bus (DVI_b) and of the whole system (WADVI). These indices are calculated using the voltage time series of the system dynamic response in post-contingency condition. The analysis of these indices allows determining the magnitude and location of FIDVR problems in power systems.

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The remainder of this paper is organized as follows. Characteristics and causes of FIDVR are presented in Section II. The proposed methodology for assessing and identifying delayed voltage recovery problems is provided in Section III. Results are obtained applying the proposed methodology in study cases in the New England 39-bus test system and these are shown in Section IV. Finally, the conclusions are presented.

II. CHARACTERISTICS AND CAUSES OF FIDVR

There are several types of loads connected to the electrical network, mainly motors, lighting equipment, and electronic devices. Particularly, the high penetration of induction motors in electricity grids is one of the most critical factors that determine the vulnerability to FIDVR events [7]. When the system's voltages are reduced under certain conditions for only three cycles, the induction motors begin to slow down and their reactive power requirement increases. As reactive power consumption increases, system voltage cannot be recovered and, in some cases, it even decreases further more [4], [5].

The small and single-phase induction motors found in the A/C equipment have low inertia and can be stalled in only a few cycles with low voltage. The larger induction motors are also prone to stall, although they are a bit slower to stop and the stall occurs for this kind of motors in a lower system voltage due to their higher inertia. The stalled induction motors have a high reactive power consumption in the transmission system, which further intensifies the initial decrease of post-fault voltage values [7].

FIDVR is a low-voltage condition initiated by a transmission or distribution fault that is characterized by:

- The stall of induction motors.
- Initial voltage recovery after the fault clearing at a level lower than 90% of the pre-contingency voltage.
- Voltage recovery in milliseconds, seconds or even minutes to reach the post-contingency steady-state voltage.

The vulnerability to a FIDVR event is also very sensitive to the location of the fault. A fault at a higher voltage level can reduce the voltage over a wider area. Therefore, the possibility that a fault reduces the voltage over a wide area, joint to a large concentration of motors in that area, are important factors that indicate the probability of occurrence of a FIDVR event [3], [12].

The determination of the location and magnitude of FIDVR problems is important to develop control strategies to mitigate delayed voltage recovery events and also to prevent a possible collapse. The effectiveness of dynamic voltage support to provide a more effective mitigation of a FIDVR event depends on the control system location and the type of control. Some possible solutions are an operation guide for the additional dispatch of generation, mainly of reactive power in the vulnerable area, secondary voltage regulation or reactive power compensation equipment operated with power electronic devices (FACTS) and installed in the vulnerable areas.

III. PROPOSED METHODOLOGY

The proposed methodology for assessing FIDVR problems is shown in the flowchart of Fig. 1. The methodology consists of six steps and allows calculating four voltage indices. The indices show the deviation of the post-disturbance voltage for a given time respect to the pre-disturbance voltage. The indices are compared with thresholds to determine buses and operating scenarios with FIDVR problems. This methodology is implemented offline using the results of time-domain dynamic simulations. The input data of the methodology are the voltage magnitude measurements in all system buses.

The implementation of the methodology allows obtaining the location of potentially vulnerable buses to FIDVR where the control actions should be focused as well as the identification of operating conditions and contingencies that alert the operator of a possible FIDVR event so as to program operating states with lower risk of FIDVR. It is important to note that with the WADVI calculation and the analysis of step 6 of this methodology, the assessment of FIDVR events can be extended to the study and analysis of contingencies. Taking into account the computational time of the methodology it can be used for the probabilistic analysis of different types of disturbances in a wide variety of load scenarios.

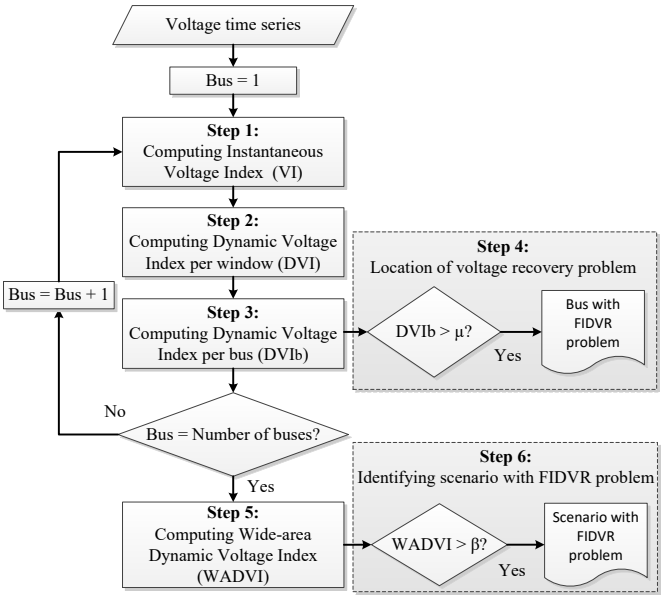


Fig. 1 Flowchart of the proposed methodology

The six steps of the methodology for assessing FIDVR events are described below:

Step 1: Calculation of the *instantaneous voltage index* (VI) for each bus. The VI measures the relative voltage deviation respect to the pre-disturbance voltage or last steady state value. The VI is calculated using (1) where: V_b^0 is the pre-disturbance voltage in a bus b, N_b is the total number of buses, t_{cl} is the fault clearing time and t_a is the analysis time. Values of voltage signal used for the VI calculation are shown in Fig. 2.

$$VI_b^t = \frac{V_b^0 - V_b^t}{V_b^0} ; \begin{cases} b \in [1, N_b] \\ t \in [t_{cl}, t_a] \end{cases} \quad (1)$$

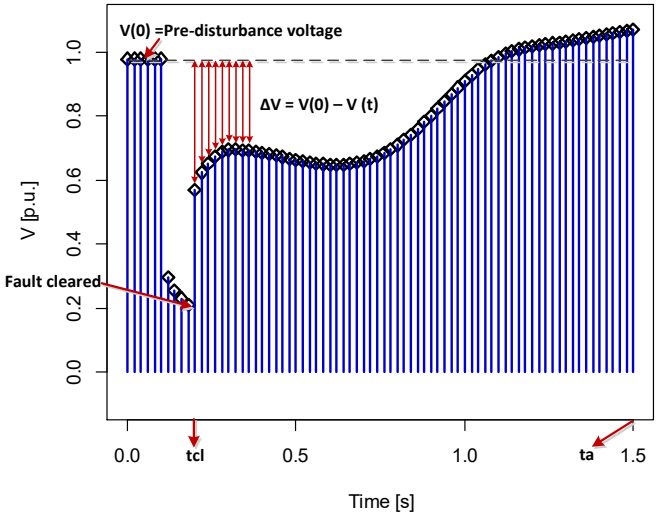


Fig. 2 Voltage time series parameters

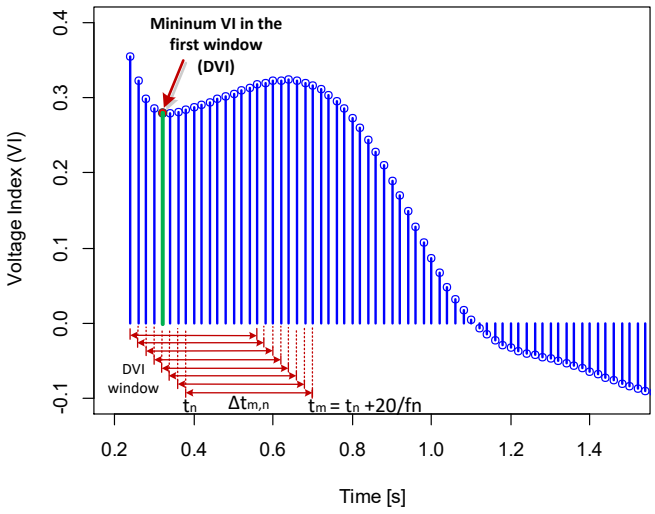


Fig. 3 Instantaneous voltage index (VI) and index per window (DVI)

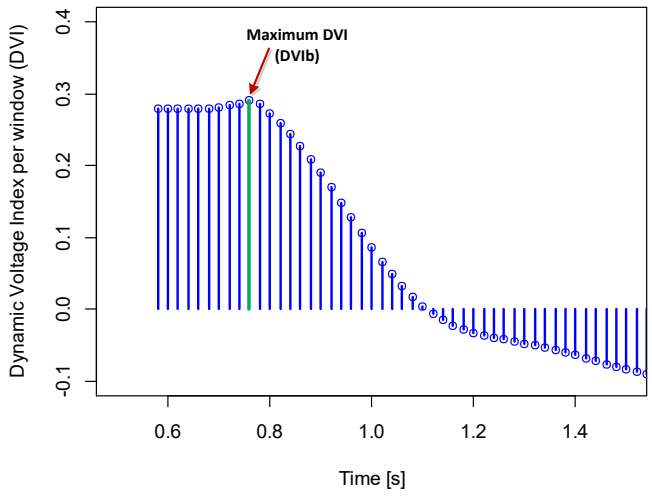


Fig. 4 Dynamic voltage index per window (DVI) and per bus (DVI_b)

Step 2: Calculation of the *dynamic voltage index per window* (DVI) for each bus. The meaning of the DVI is the value below which the relative voltage is maintained for a specific number of cycles. The mobile time window (Δt) is determined with (2) to compute the DVI and the extension of the window is defined considering the criterion of the number of cycles according to the industrial criterion of [11], which is 20 cycles of nominal frequency. The parameters of the voltage profile for calculating the DVI and the representation of the mobile time window are shown in Fig. 3. The DVI index per window is the minimum value of the VI values in that period. The DVI is calculated using (3), obtaining a DVI value per window of the time series, as shown in Fig. 4.

$$\tau = 20 * 1/f_{nom} \;=\; \Delta t_{m,n} = t_n - t_m \tag{2}$$

$$DVI_b^{\Delta t_{m,n}} = \min\, VI_b^t\,; \begin{cases} t \in [t_m, t_n] \\ t_m, t_n \in \begin{bmatrix} (t_{cl}, t_{cl}+\tau), \\ (t_a-\tau, t_a) \end{bmatrix} \end{cases} \tag{3}$$

Step 3: Calculation of the *dynamic voltage index per bus* (DVI_b) applying (4), which is the maximum DVI value of all windows that were computed in the step 2.

$$DVI_b = \max DVI_b^{\Delta t_{m,n}} \tag{4}$$

Step 4: Location of FIDVR problems using the index DVI_b. The DVI_b is compared to a bus voltage recovery threshold (μ) and the buses with a DVI_b higher than μ are classified as the buses with FIDVR problems.

Step 5: Calculation of the *wide-area dynamic voltage index* (WADVI) or index of the whole system with (5). The WADVI is determined with the maximum DVI_b value of all system buses.

$$WADVI = \max_{1 \le b \le N_b} DVI_b \tag{5}$$

Step 6: Identification of scenarios with FIDVR problems using the WADVI value, which is compared to a system voltage recovery threshold (β). The characterization of the scenarios allows determining the system operating conditions and contingencies in which FIDVR can be manifested.

IV. Simulation Results

A. Description of study cases

The developed methodology is tested in the New England 39-bus test system. In the modeling of the test system, dynamic components are included, such as the governors of generators, AVRs, and the aggregate load model shown in Fig. 5. The time-domain dynamic simulations are conducted in the DigSILENT Power Factory program.

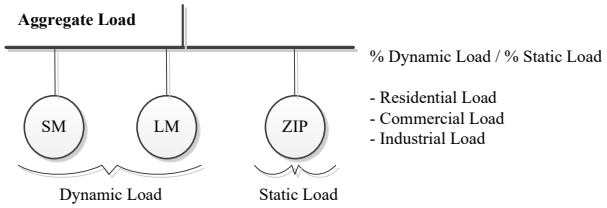


Fig. 5 Aggregate load model

Study cases are analyzed considering different proportions of static and dynamic loads such as large and small motors, to model residential, commercial and industrial load. It was considered the fault clearing time of 0.1 s, the simulation time of 10 s and the integration step of 0.02 s. The voltage profiles of the system response under a fault in a transmission line and its subsequent clearance for two study cases are shown in Fig. 6; (a) study case 1 is a fault on the line 14-15, (b) study case 2 is a fault on the line 17-27. In case 1 it is observed that in the first seconds after the fault clearing the bus voltages do not recover to their pre-contingency value, and the voltage decreases until reaching values below 0.7 pu, while in case 2 the voltage reaches values close to 0.8 pu and then recovers with a damped response.

B. Application of the proposed methodology in the New England 39-bus test system

1) Study case 1

The first step, the voltage index (VI) for all buses and each sample of the time series is calculated with (1). Results of the VI calculation for all buses are shown in Fig. 7. It is observed that the voltage deviation respect to the pre-disturbance voltage for buses 15 to 19 reaches VI values close to 0.4 in 1.5 s of the simulation.

Subsequently, step 2 is performed, using a mobile window of 333 ms in which the integration step (20 ms) is equivalent to 17 samples. The dynamic voltage index (DVI) for all buses and each window is calculated with (3). The DVI calculation in comparison with the VI allows obtaining a voltage deviation value that remains in time, which is one of the causes of problems in power equipment instead of the instantaneous deviations. The result of the DVI calculation for all buses of study case 1 is shown in Fig. 8. It is observed that some buses have high values of voltage deviation, higher than 0.3, during the first two seconds. This deviation is considered as unacceptable deviation by some network operators that have a reference value of 0.2 [11].

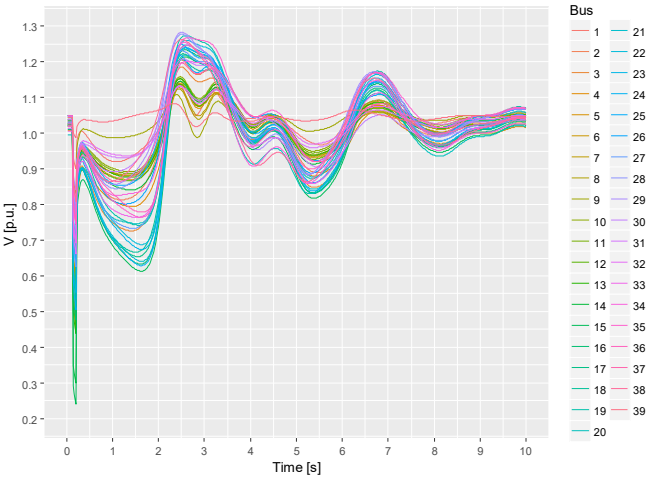
In step 3, the dynamic voltage index per bus (DVI_b) is calculated with (4), which is the maximum value of the DVI. Calculation results are shown in Fig. 9, where it can be observed that those buses with the highest index values correspond to buses 15-18, 21 and 24.

In step 4, buses with FIDVR problems are identified, the limit values proposed in [11] $\mu = \beta = 0.2$ are considered for this analysis. From the analysis in Fig. 9, it is determined that buses 2-4, 15-24, 26, 27, 33, 35 and 36 have FIDVR problems.

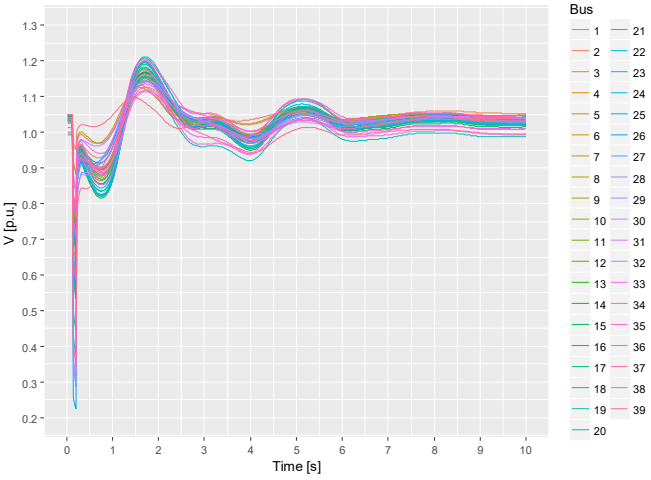
In step 5, the WADVI is calculated with (5), which represents the magnitude of the problem in the system and it is observed in Fig. 9 as the highest value of DVI. The WADVI for this case is 0.3796 located in bus 15.

In step 6, it is analyzed whether the operating scenario has FIDVR problem, the result shows that the value of the WADVI (0.3796) is higher than β (0.2) therefore it has FIDVR problem.

The computational time to calculate the indices in the test system using a computer with an AMD Athlon ™ II X4 3 GHz processor and 4 GB RAM is 131 ms.



(a)



(b)

Fig. 6 Voltage profiles in the New England 39-bus test system. (a) Study case 1. (b) Study case 2

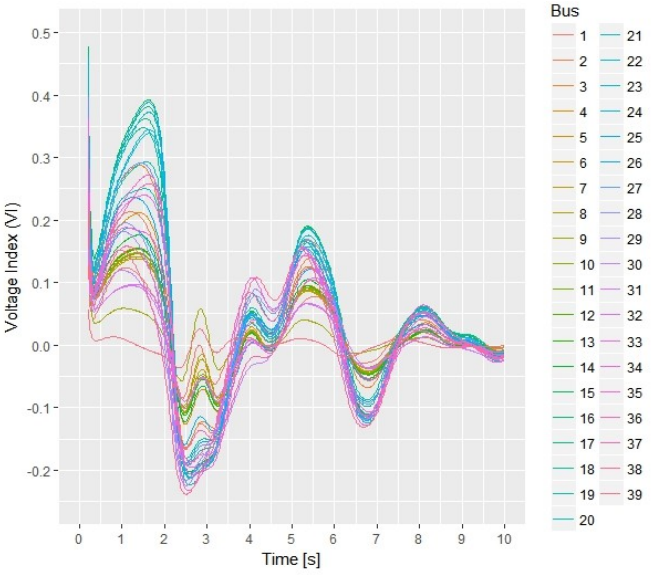


Fig. 7 Voltage index (VI) for the 39 buses

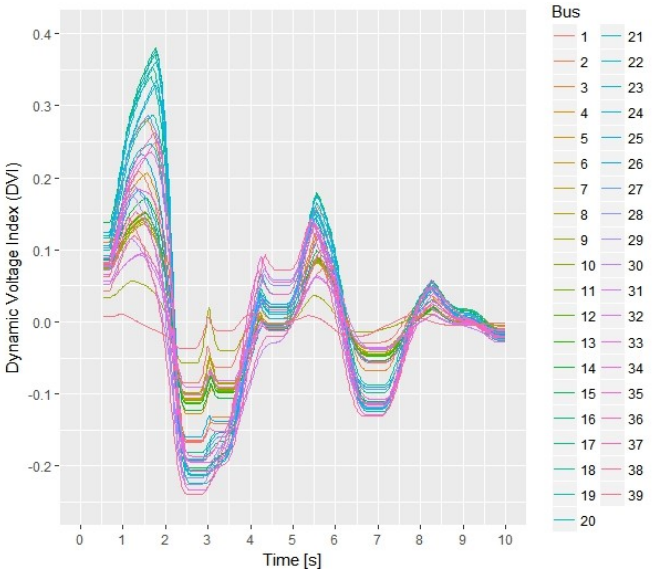


Fig. 8 Dynamic voltage index (DVI) for the 39 buses

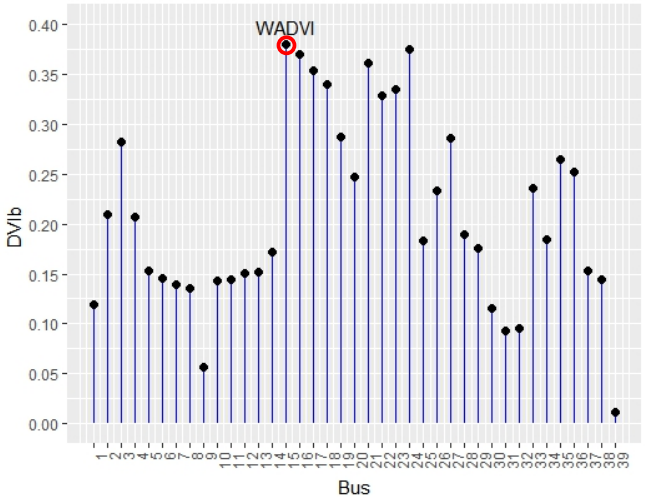


Fig. 9 Dynamic voltage index per bus (DVI_b) and WADVI

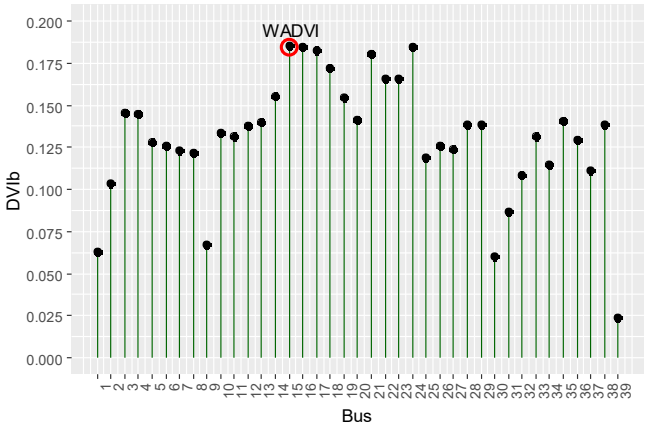


Fig. 10 DVI_b and WADVI of study case 2

2) Study case 2

Steps 1-3 of the methodology are followed in the analysis of the study case 2. The result of the DVI_b calculation in step 3 is shown in Fig. 10. In step 4, when comparing DVI_b with μ, there is no bus with FIDVR problem. In step 5, the WADVI is calculated, the result is 0.185. In step 6 it is determined that the operating scenario of case 2 has no FIDVR problem because the WADVI is lower than β (0.2).

V. CONCLUSIONS

A new methodology for assessing and identifying fault-induced delayed voltage recovery (FIDVR) problems based on dynamic voltage indices was presented. Dynamic indices are calculated for each bus and in the whole system, which allows determining both buses and scenarios vulnerable to a FIDRV event. The results of the study cases showed the ability of the methodology to identify, quantify and even locate voltage recovery problems using these proposed indices. The determination of the location and magnitude of FIDVR problems allows proposing control strategies based on dynamic voltage support devices that mitigate the occurrence or consequences of voltage recovery events, preventing a possible collapse. The methodology proposed in this paper is simple and with low computational time, which makes possible its implementation in probabilistic contingency studies with a wide variety of operating conditions.

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