D-Band Frequency Quadruplers in BiCMOS Technology

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***Abstract*— This paper presents two D-band frequency quadruplers (FQs) employing different circuit techniques. First FQ is a 129–171-GHz stacked Gilbert-cell multiplier using a bootstrapping technique, which improves the bandwidth and the conversion gain with respect to the conventional topology. Stacked architecture enables current reuse for the second frequency doubler resulting in a compact and energy-efficient design. The circuit reaches 3-dB bandwidth of 42 GHz, which is the highest among similar reported quadruplers. It achieves 2.2-dBm saturated output power, 5-dB peak conversion gain, and 1.7% peak DC-to-RF efficiency. The stacked FQ occupies 0.08 mm^2 and consumes 22.7 mA from 4.4-V supply. Second presented circuit is a transformer-based injection-locked FQ (T-ILFQ) employing an E-band push–push voltage-controlled oscillator (PP-VCO). The VCO is a self-buffered common-collector Colpitts oscillator with a transformer formed on emitter inductors. Proposed configuration does not reduce the tuning range of the VCO, thus providing wide locking range and high sensitivity with respect to the injected signal. The T-ILFQ achieves 21.1% locking range, which is the highest among other reported injection-locked frequency multipliers. The peak output power is −4 dBm and the input sensitivity reaches −22 dBm. The circuit occupies 0.09 mm^2 and consumes 14.8 mA from 3.3-V supply.**

***Index Terms*— D-band, Gilbert cell (GC), injection locked, push–push (PP), quadrupler, stacked, transformer, voltage-controlled oscillator (VCO), wideband.**

I. Introduction

SILICON-GERMANIUM technology proved to be a good candidate for integrated mm-wave and sub-THz communication systems and radar sensors [1], [2]. It offers a full integration of high-frequency modules with digital blocks at moderate mask costs compared to III–V-compound-semiconductor technologies.

Manuscript received January 5, 2018; revised March 10, 2018 and May 16, 2018; accepted May 22, 2018. This paper was approved by Guest Editor Hua Wang. This work was supported by the German Federal Ministry of Education and Research (BMBF) as a part of the EMPHASE Research Project, in which an integrated energy-efficient multiprocessor platform for autonomous electric driving is developed. *(Corresponding author: Maciej Kucharski.)*

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Digital Object Identifier 10.1109/JSSC.2018.2843332

Most of the modern high-performance mm-wave transceivers contain a local oscillator (LO) generation circuit that provides a stable signal for the transmitting and receiving (TX/RX) modules. This is typically implemented with a phase-locked loop (PLL) that stabilizes a voltage-controlled oscillator (VCO). The signal generated by the VCO is chosen in the frequency range, where a low phase noise and wide tuning range can be achieved. This is typically a compromise between the optimum resonant tank quality factor, transistor performance, and a number of multiplying stages required to translate the signal to the frequency requested by the TX/RX modules. The use of frequency multipliers enables generation of stable high-frequency signals with a phase noise determined by the low-frequency source. However, beyond f_T/f_{MAX}, free-running harmonic power sources might be the right solution for power generation [34].

This paper presents two D-band frequency quadruplers (FQs) using different circuit techniques. Both approaches are analyzed and compared. Furthermore, design aspects and tradeoffs are discussed. In Section II, a wideband stacked Gilbert-cell (GC) FQ using a bootstrapping technique is described. Section III presents a transformer-based injection-locked FQ (T-ILFQ) with wide locking range. Both circuits are summarized and compared with the earlier reported publication in Section IV.

II. Stacked Bootstrapped Gilbert-Cell Frequency Quadrupler

The most convenient way to realize a frequency quadrupling is to cascade or stack frequency doublers [3]–[6]. There are basically two techniques used to double the frequency. First employs a GC to mix the input frequency with itself, thus producing a signal at the doubled frequency. Another technique is based on even harmonics superposition [so-called push–push (PP) doublers]. However, PP-doublers have inherently single-ended output, which makes them not favorable in fully differential designs. Cascading two PP frequency doublers requires an interstage balun in order to generate differential signals to drive the second stage [7]. Another way is to drive two PP doublers with quadrature signals in order to obtain a balanced signal that feeds the second stage [8]. This implies the use of additional circuitry for quadrature signals' generation, which inflicts more difficulties in the design process. On the other hand, PP technique, if combined with injection-locked VCO (IL-VCO), can be successfully

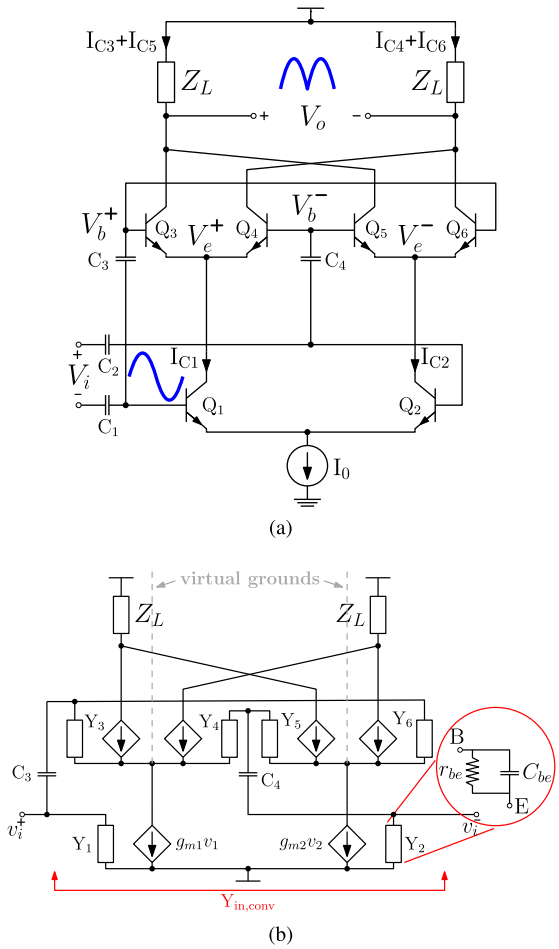


Fig. 1. (a) Conventional GC frequency doubler topology. (b) Small-signal model.

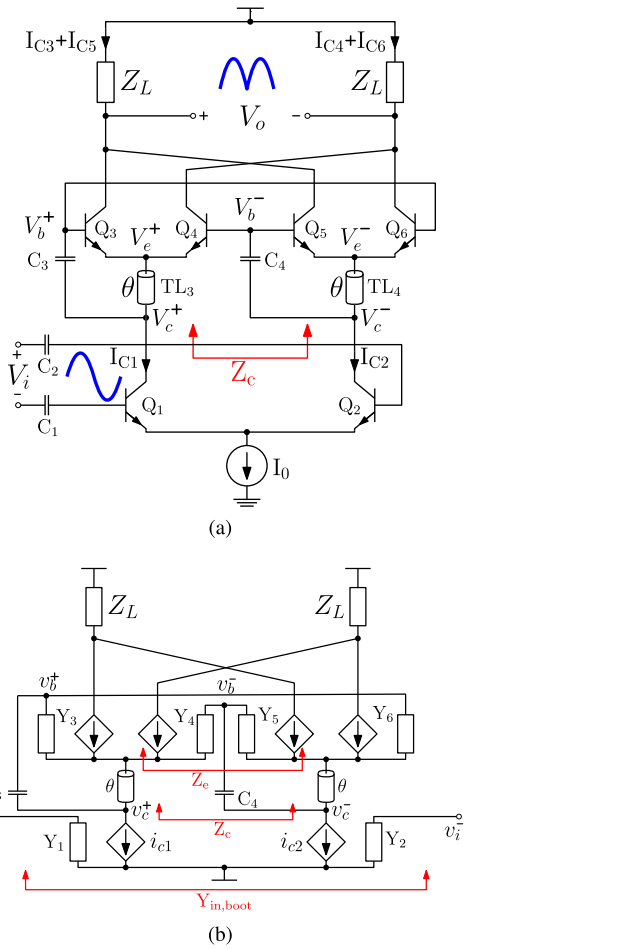


Fig. 2. (a) Bootstrapped topology. The signal driving the switching quad is taken from Q_{1-2} collectors. (b) Small-signal model.

used for frequency multiplication above f_T/f_{MAX} of the transistors [20]. In addition, it gives possibility to tune the phase of the output signal, which is a very attractive feature regarding phased-array applications.

A. Circuit Analysis

Fig. 1(a) shows a conventional frequency doubler based on a GC. Q_{1-2} forms a transconductance stage. The collector currents I_{C1-C2} become emitter currents of Q_{3-6}, which perform the self-mixing operation since they are driven at the same rate as the input signal. Next, we perform an analysis to derive the conversion gain of that frequency doubler. Assuming that the saturation and base currents are negligible, the tail current source is ideal, and that the output resistances in the transistors are infinite [10], we obtain

$$V_o = I_0 Z_L \tanh\left(\frac{V_i}{2V_T}\right)\tanh\left(\frac{V_b}{2V_T}\right). \tag{1}$$

Next, noticing that $\tanh(x) \approx x$ for $x \ll 1$ we rewrite (1) as follows:

$$V_o = I_0 Z_L \left(\frac{V_i}{2V_T}\right)\left(\frac{V_b}{2V_T}\right) \tag{2}$$

which holds true as long as $V_i, V_b \ll 2V_T$. This assumption is justified since, unlike in case of a mixer, V_b greatly depends on V_i and can be considered small with respect to $2V_T$. In the conventional frequency doubler $v_b = v_i$ assuming that the capacitors C_{3-4} are perfect DC blockers. Then, (2) simplifies to

$$v_o = \frac{I_0 Z_L}{4V_T^2} v_i^2. \tag{3}$$

Let us consider v_i to be a monotone excitation

$$v_i = V_i \cos(\omega_i t + \varphi_0) \tag{4}$$

where V_i is the small-signal amplitude, ω_i is the input angular frequency, and φ_0 denotes the initial phase, which for the moment can be considered to be zero. Then, the small-signal output voltage reads

$$v_o = \frac{g_m Z_L V_i^2}{4V_T}(1 + \cos 2\omega_i t) \tag{5}$$

where we used relation $g_m = I_{C1}/V_T = I_{C2}/V_T = I_0/2V_T$. Since all transistors have the same sizes but differ in quiescent collector current, $g_{m1} = g_{m2} = g_m$ and $g_{m3} = g_{m4} = g_{m5} = g_{m6} = g_m/2$ due to halved I_{C1} and I_{C2} between Q_{3-4} and Q_{5-6}, respectively. From (5), we see that the output signal contains a component with doubled frequency and a DC part. Also, assuming the same input and output terminations, the output power depends quadratically with respect to the

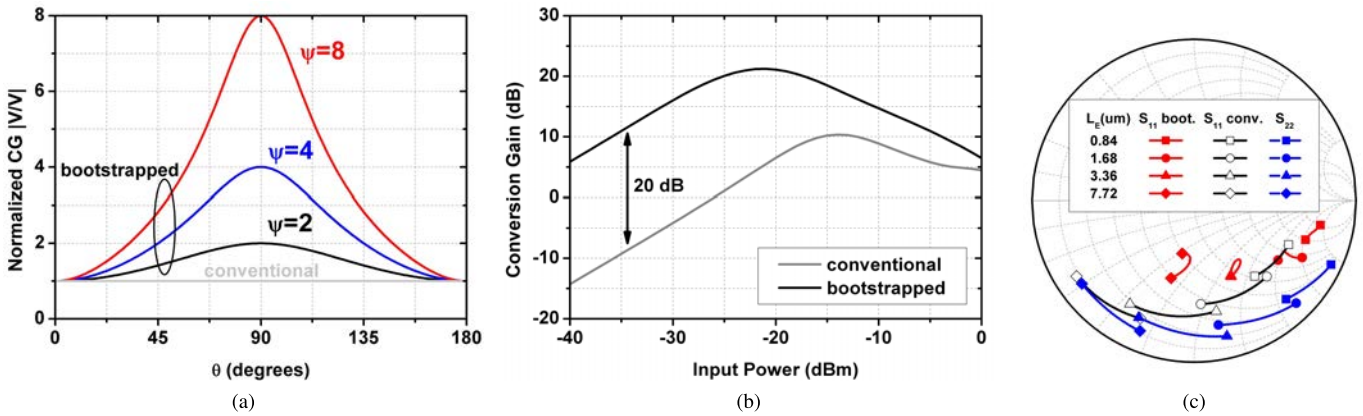


Fig. 3. (a) Normalized small-signal voltage conversion gain of a conventional and bootstrapped doubler versus θ for different $\Psi = (g_m Z_0)^2$ values. (b) Example of simulated conversion gain of a conventional and bootstrapped frequency doubler with lossless matching networks. (c) Simulated input and output reflection coefficient of a conventional and bootstrapped FQ for a different transistor size.

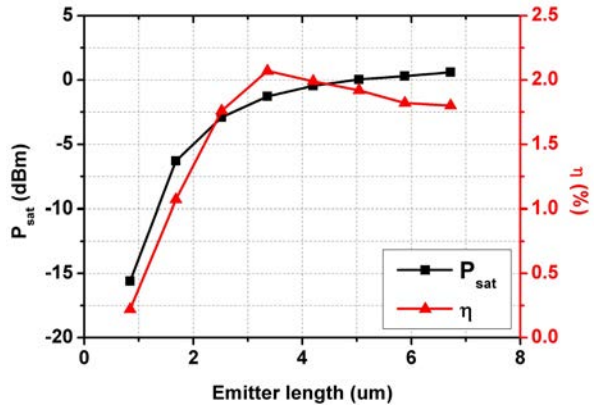


Fig. 4. Simulated saturated output power and DC-to-RF efficiency versus transistor size.

input power. Considering only the desired component at $2\omega_i$, it follows:

$$V_o = \frac{g_m Z_L V_i^2}{4V_T} \tag{6}$$

and the small-signal voltage conversion gain reads

$$\mathrm{CG}_v = V_o/V_i = V_i \frac{g_m Z_L}{4V_T}. \tag{7}$$

Note that the conversion gain is a function of the input voltage. This is expected since the output voltage is a function of the input voltage squared. A small-signal equivalent circuit of the conventional frequency doubler is shown in Fig. 1(b). A few assumptions are made to simplify the analysis. We consider the collector–emitter output resistance r_o to be infinite, as well as the parasitic capacitances C_{bc} and C_{ce} to be negligibly small. We leave C_{be} as typically the largest in the transistor. Note that as C_{bc} increases, the input Miller capacitance may become significant, which for high-voltage gain will affect the input impedance. Next, we assume the devices Q_{1-6} to have the same size (thus the same r_{be} and C_{be}). Exploiting the virtual ground at the emitters of Q_{3-4} and Q_{5-6}, the differential input admittance $Y_{\mathrm{in,conv}}$ reads

$$\left(\frac{Y_1}{1+Y_1/j\omega C_3} + Y_3 + Y_6\right) \Big\| \left(\frac{Y_2}{1+Y_2/j\omega C_4} + Y_4 + Y_5\right). \tag{8}$$

Treating C_{3-4} as perfect DC-blocks and assuming that admittances Y_{1-6} are equal, it follows:

$$Y_{\mathrm{in,conv}} = \frac{3}{2} Y_1. \tag{9}$$

Let us now investigate the conversion gain and input admittance of a bootstrapped frequency doubler [see Fig. 2(a)]. Since the base voltage is taken from Q_{1-2} collectors, $v_b = v_c$ assuming that C_{3-4} are infinite. In order to use (3) for obtaining the conversion gain, we notice that

$$v_b = v_c = (i_{c1} - i_{c2}) Z_c = g_m v_i Z_c \tag{10}$$

where Z_c is a transformed impedance Z_e presented by Q_{3-6} emitters

$$Z_e \approx \frac{1}{g_m} \tag{11}$$

assuming that $Y_{3-6} \ll g_m$ and noticing that g_m of Q_{3-6} is two times smaller than that of Q_{1-2} since I_{C1} is equally divided between Q_3 and Q_5. Z_c reads

$$Z_c = Z_0 \frac{Z_e + j Z_0 \tan(\theta)}{Z_0 + j Z_e \tan(\theta)} \tag{12}$$

where Z_0 is the characteristic impedance and θ is the length of TL_{3-4}. Combining (12) and (10) gives

$$v_b = g_m v_i Z_0 \frac{Z_e + j Z_0 \tan(\theta)}{Z_0 + j Z_e \tan(\theta)}. \tag{13}$$

Using (4), we express v_b with respect to v_i as follows:

$$v_b = V_i g_m Z_c \cos(\omega_i t + \varphi_0). \tag{14}$$

Using (3), (4), and (14) and assuming $\varphi_0 = 0$, we obtain

$$v_o = \frac{g_m Z_L V_i^2}{4V_T} g_m Z_c (\cos(2\omega_i t)). \tag{15}$$

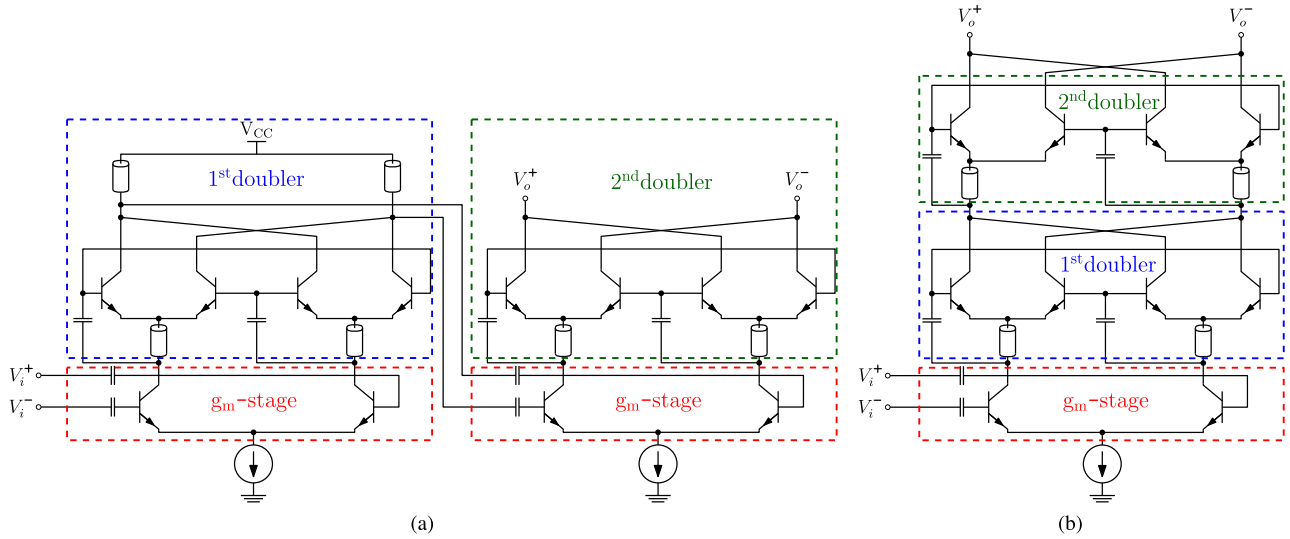


Fig. 5. FQ formed with (a) two cascaded and (b) two stacked frequency doublers.

As previously, by extracting from (15) a component at $2\omega_i$ we define a small-signal conversion gain

$$\mathrm{CG}_v = V_o/V_i = V_i \frac{g_m Z_L}{4V_T} g_m Z_c. \tag{16}$$

Comparing (7) and (17), we obtain

$$\mathrm{CG}_{v,\mathrm{boot}} = \mathrm{CG}_{v,\mathrm{conv}} g_m Z_c. \tag{17}$$

Let us consider two cases. If there is no TL_{3-4}, $\theta = 0°$ and $Z_c = Z_e = 1/g_m$. Then, using (17) results in

$$\mathrm{CG}_{v,\mathrm{boot}} = \mathrm{CG}_{v,\mathrm{conv}}. \tag{18}$$

The small-signal voltage conversion gain is equal for both configurations, if no delay between V_b and V_e is introduced. Let us investigate the case, when $\theta = 90°$. From (17) and (12), we obtain

$$\mathrm{CG}_{v,\mathrm{boot}} = \mathrm{CG}_{v,\mathrm{conv}} (g_m Z_0)^2. \tag{19}$$

The above considerations show that $\mathrm{CG}_{v,\mathrm{boot}}$ can be enhanced with respect to $\mathrm{CG}_{v,\mathrm{conv}}$ provided that the factor $Z_0 > 1/g_m$. Also, the inclusion of TL_{3-4} minimizes the DC component in the output signal, which for $\theta = 90°$ is equal to zero. The influence of the DC component and a problem of imbalance at the output in general are discussed in [9]. Fig. 3(a) shows the derived conversion gain of the conventional and bootstrapped frequency doubler. Tuning the length of TL_{3-4} can enhance the gain of the bootstrapped doubler with respect to conventional one. Also, the DC component resulting from the self-mixing can be simultaneously minimized. Note that the above analysis does not account for the input impedance seen at the bases of the switching. This finite impedance limits the possible conversion gain improvement, since it shunts $\mathrm{Z_c}$. Fig. 3(b) shows a conversion gain example for a conventional and bootstrapped doubler. In this simulation, the source and load terminations were matched to the input and output impedances of the circuit resulting in a lossless power transfer from the source to the device and from the output to the load. Both circuits have the same-sized transistors with four fingers each ($L_E = 3.36\ \mu$m). The bootstrapped doubler has also TL_{3-4} with optimized theta for the highest conversion gain. For low input power ($V_i, V_b \ll 2V_T$), the conversion gain increases linearly with respect to the input power. Here, $Z_0 = 40\ \Omega$ and $g_m = 100$ mS resulting in $\Psi = 16$, which corresponds to $\Psi \approx 24$ dB. The simulated conversion gain for the bootstrapped doubler is around 20 dB higher than for the conventional one under the small signal conditions. The difference between the calculated and simulated values comes from neglecting many factors in the analysis. Nevertheless, the advantage of the bootstrapped topology over the conventional one is clearly visible. As the input power increases, the conversion gain starts to compress and eventually it starts to decrease for high input-power levels. Since the frequency doubler is typically operated with high input power, large signal simulations were performed to obtain a fair comparison between the architectures [see Fig. 3(b)].

The input admittance of the bootstrapped frequency doubler is determined only by the input transistors Q_{1-2} and is given by

$$Y_{\mathrm{in,boot}} = \frac{1}{2} Y_1 = \frac{1}{3} Y_{\mathrm{in,conv}}. \tag{20}$$

Note that the input admittance of a bootstrapped doubler is three times lower with respect to the conventional architecture, which was confirmed in small-signal simulation of both structures. Fig. 3(c) presents input and output reflection coefficients in 25–55- and 100–220 GHz range, respectively, for different emitter lengths L_E. In this simulation, we kept the size of Q_{1-6} equal so that all transistors have the same r_{be} and C_{be}. Due to less sensitive change of S_{11} over the frequency in case of a bootstrapped frequency doubler, we should expect this topology to have larger bandwidth with respect to the conventional architecture. Note that the change of S_{22} over the frequency is more sensitive than the change of S_{11} (for a bootstrapped doubler), meaning that the circuit is bandwidth limited at the output.

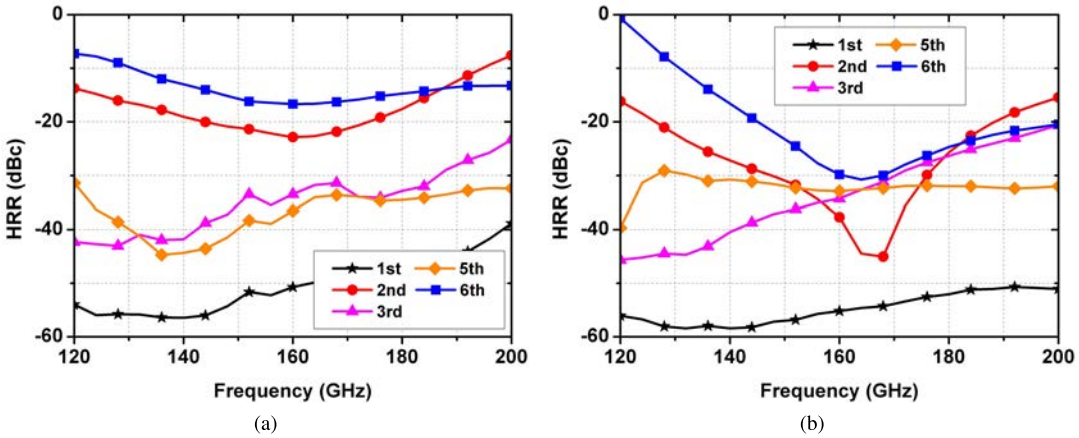


Fig. 6. Simulated HRR. (a) Without tail resistor. (b) With tail resistor.

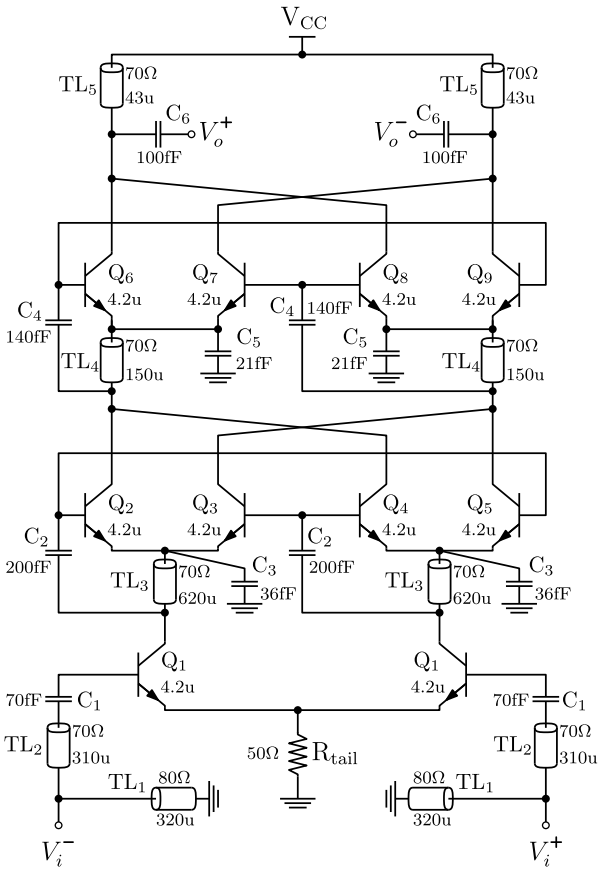


Fig. 7. Schematic of the stacked bootstrapped GC FQ.

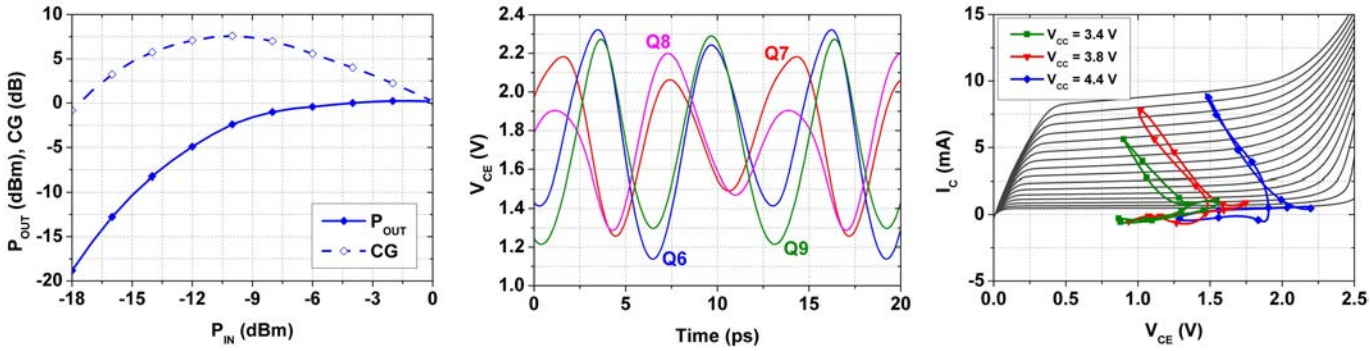
B. Circuit Implementation

Instead of cascading two frequency doublers, a stacked topology is proposed for wider bandwidth and less area consumption. Although it requires higher supply voltage, it has an advantage in terms of bandwidth and compactness. Since a cascaded FQ consists of two branches, which must be DC-decoupled, it requires an interstage matching network, thus limiting the bandwidth, introducing more losses, and having a negative impact on the circuit size. It also dictates using more complex biasing, since the stages must be DC-decoupled.

In order to optimize the FQ for bandwidth and output power, the transistor size has been varied at the constant optimum emitter current density $J_{E_{\text{opt}}} \approx 1.2$ mA/um for the highest f_T/f_{MAX}. Power handling capabilities of a transistor can be improved by increasing its size. Fig. 4 shows simulated saturated output power and RF-to-DC efficiency of a stacked FQ (Fig. 5) for different emitter sizes of the available transistors. The IHP technology offers discretely scalable HBTs with a maximum number of eight fingers for a single device. A five-finger transistor has been chosen as a compromise between maximum output power and RF-to-DC efficiency, which corresponds to 4.2 μm emitter length. The analysis presented in Section II-A does not account for transistor parasitics and an EM simulation must be performed to obtain the optimum TL_{3-4} length. Also, DC-decoupling capacitors [C_{3-4} in Fig. 2(a)] change the optimum theta. The choice of C_{3-4} is dictated by their resonant frequency (determines the upper limit) and layout restrictions. In order to keep the layout compact, C_{3-4} should be small but still large enough not to impact the signal. Here, we chose 200 fF to be used. According to simulations, the phase of V_b is ahead of V_e by approximately 10° (at 40 GHz), which makes the optimum theta less than 90°. After EM simulation, the optimum theta appeared to be approximately 60°, which is beneficial from the layout point of view. The TL_{3-4} characteristic impedance Z_0 was chosen to be 70Ω, and $g_m = 170$ and 85 mS for Q_1 and Q_{2-9}, respectively, which satisfies $Z_0 > 1/g_m$ condition.

Fig. 6(a) shows the simulated harmonic rejection ratio (HRR) of the stacked FQ without a tail resistor in the g_m-stage. The second and the sixth harmonics have visibly higher level than the other harmonics. The second harmonic current caused by the transistor nonlinearity not only leaks to the output, but it is also doubled and self-mixed in the switching quad. Adding a tail resistor in the g_m-stage improves the second and the sixth HRR by more than 10 dB in 150–180 GHz range [see Fig. 6(b)], since it introduces a degeneration for common-mode signals, especially the second harmonic.

The schematic of the optimized stacked FQ is presented in Fig. 7. Current mirrors (not shown) were used to generate DC voltage bias for the core transistors. TL_3 and TL_4



(a) (b) (c)

Fig. 8. (a) Simulated output power and conversion gain for $V_{CC} = 4.4$ V. (b) Simulated V_{CE} waveforms P_{sat} of Q_{6-9} for $V_{CC} = 4.4$ V. (c) Dynamic load line of Q_6 for different V_{CC} values.

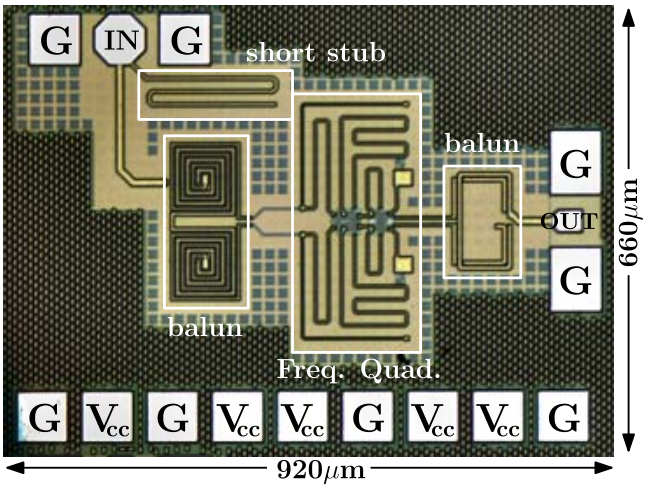
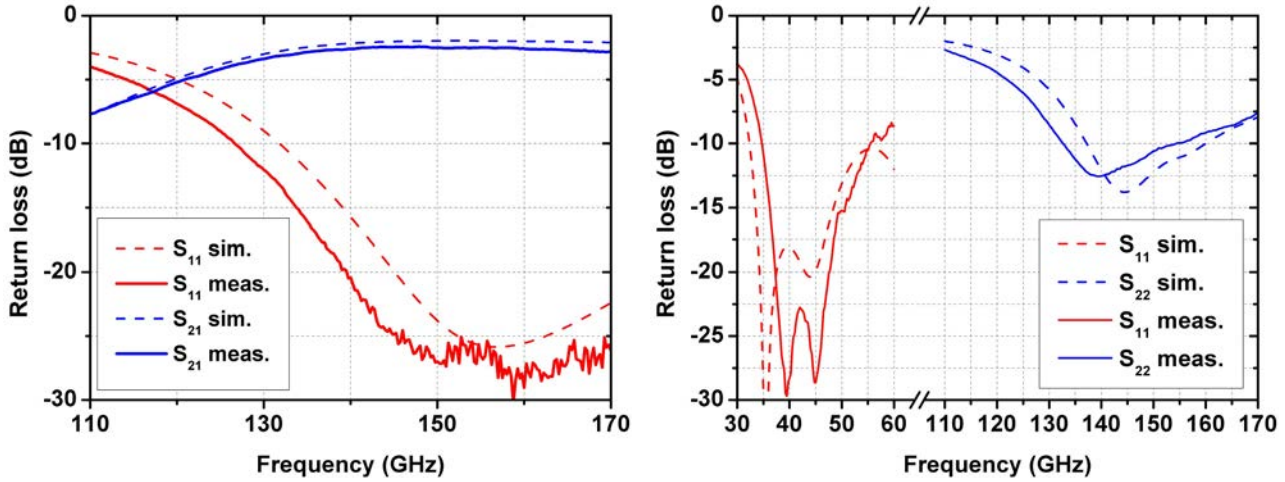


Fig. 9. Chip micrograph.

introduce a delay for higher voltage swing at the switching quad and thus higher conversion gain. Small C_3 and C_5 help to increase HRR by shunting higher harmonics to ground while having a negligible effect on the fundamental signal and optimum theta. TL_1, TL_2, C_1 and TL_5, C_6 match the impedance to 100 Ω at the input and output, respectively. Fig. 8(a) presents simulated output power and conversion gain versus input power for $V_{CC} = 4.4$ V. Due to high supply voltage, the device reliability was investigated. The simulated V_{CE} waveforms [see Fig. 8(b)] show that V_{CE} cyclically goes beyond $BV_{CE0} = 1.7$ V. However, BV_{CE0} is defined in case of an open base terminal, which represents the worst possible conditions with respect to device reliability. Here, the DC impedance presented at the bases of Q_{6-9} is around 1 kΩ, which shifts BV_{CE} beyond 2.5 V. Also, as shown in Fig. 8(c), large V_{CE} occurs at low collector currents, meaning that the device is driven within the safe region.

C. Measurement Results

A stacked GC FQ was fabricated in a SiGe 130 nm BiCMOS technology using a SG13G2 process of IHP [11]. The transistors achieve $f_T/f_{MAX} = 300/500$ GHz and have collector–emitter breakdown voltage $BV_{CE0} = 1.7$ V. The die micrograph is presented in Fig. 9. The circuit occupies 0.61 mm^2, including bondpads and baluns. The size of the stand-alone FQ is only 0.08 mm^2. A back-to-back Q-band and D-band Marchand baluns have been designed and measured in order to convert differential signals to single-ended format. Measured input return loss and transmission of the D-band balun is shown in Fig. 10(a). The input and output return loss of the FQ is shown in Fig. 10(b). Disregarding a slight shift toward lower frequencies, there is good agreement between simulated and measured values. Fig. 11 shows the measured saturated output power versus frequency. An external signal source was used to generate 2.5 dBm driving signal in 30–45 GHz range. The output power was measured for three different supply voltages using a VDI Erickson PM5 power meter. At 4.4 V, the circuit achieves maximum output power of 2.2 dBm and 3-dB bandwidth of 42 GHz. Fig. 12 presents the output power and conversion gain versus input power at 155 GHz for three different voltage supplies. At 4.4 V, the circuit achieves 5 dB conversion gain and saturates at 2.2 dBm output power. At 3.4 V, the quadrupler has still a positive conversion gain of 2.5 dB and saturates at −4 dBm output power. Fig. 13 shows the efficiency of the FQ defined as a ratio of the RF output power to the DC power consumption (η) together with efficiency accounting for the input power defined as $PAE = (P_{out} - P_{in})/P_{DC}$. Also, we plotted the highest simulated η, which occurred for the supply voltage of 3.4 V. Increasing the supply voltage in simulation did not necessarily led to a better efficiency, which is probably due to inaccurate large-signal models of a transistor. Hypothetically, η could be further enhanced by removing the tail resistor but probably it would not exceed 2.5%. At 4.4 V, the presented circuit achieves 1.7% DC-to-RF efficiency and 0.9% PAE at 155 GHz. Fig. 14 presents a measured harmonic spur rejection defined as the power ratio of an unwanted harmonic signal to the desired fourth harmonic. In order to measure harmonic signals, different measurement setups were used. The leaked fundamental signal was measured directly using a 50 GHz E4448A spectrum analyzer from Agilent. For the second and the third harmonic, E-band and F-band setups were used, including waveguide sections and subharmonic mixers.



(a) (b)

Fig. 10. (a) Measured input return loss and transmission of the D-band Marchand balun. (b) Measured input and output return losses of the stacked FQ.

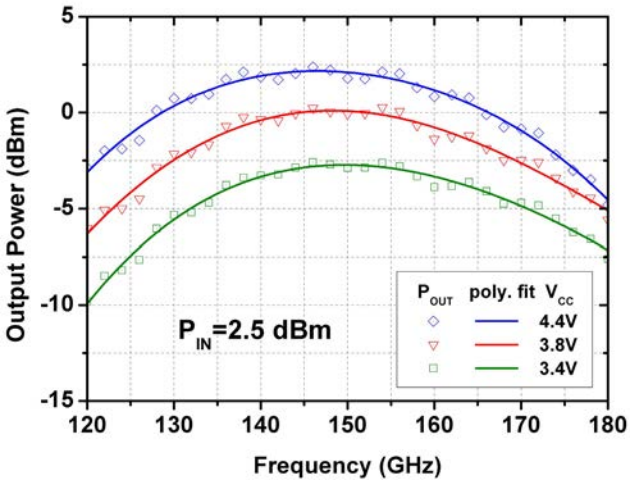


Fig. 11. Measured output power versus frequency for different supply voltages.

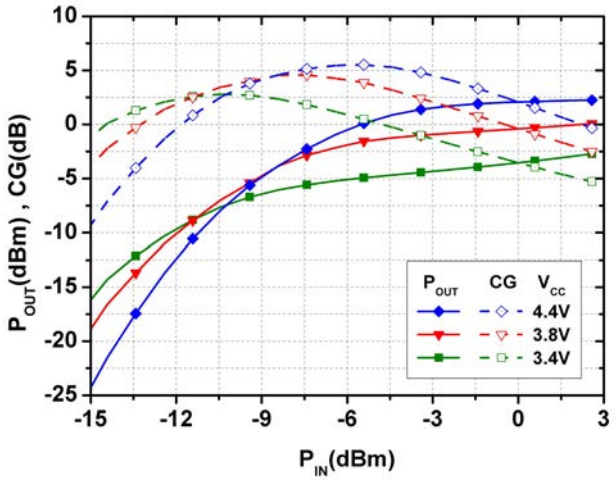


Fig. 12. Measured output power and conversion gain at 155 GHz versus input power for different supply voltages.

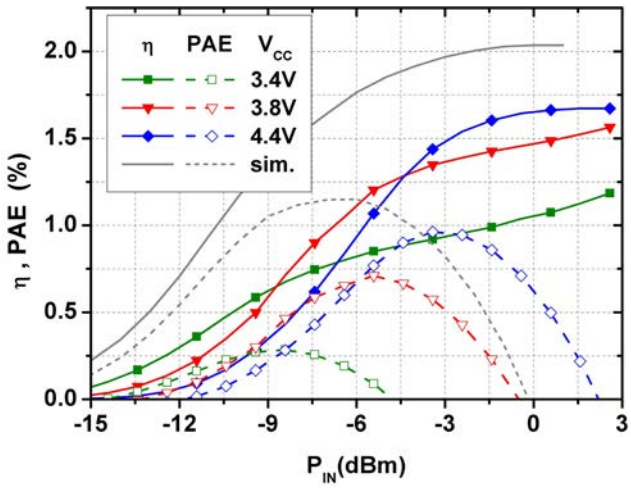


Fig. 13. Measured efficiency at 155 GHz versus input power for different supply voltages.

In 129–171 GHz range, the unwanted harmonic leakage is well below −20 dBc with respect to the fourth harmonic. Differences between simulated and measured values of HRR can be due to fact that in simulation, it is not possible to capture coupling occurring through the substrate. Unfortunately, due to the lack of measurement equipment, higher harmonics could not be measured.

III. Transformer-Based Injection-Locked Frequency Quadrupler

Another group of frequency multipliers are based on injection-locking phenomenon, which has been studied since 1946 [12]. Injection-locked oscillators (ILOs) drew attention in recent years due to high-efficiency and low-power potential in clock recovery systems [13], [14]. An ILO can serve as a frequency multiplier, if it is locked by a harmonic of an injected signal. Since the oscillator is a self-regenerating circuit, it is expected to provide constant output power at very low input-power levels. In locked state, the oscillator tracks the phase of the injected signal, providing a clean and stable output signal [13]. Also, IL-VCOs enable phase tuning, which is very attractive for phased-array

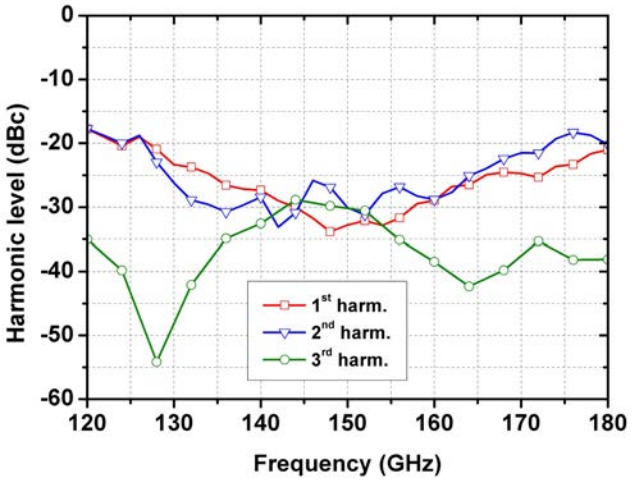


Fig. 14. Measured harmonic spur rejection of the FQ.

applications. Until now, mostly injection-locked frequency triplers (ILFTs) [15]–[18] have been reported, whereas only a few frequency doublers or quadruplers can be found in the literature [19], [20].

A. VCO

Generation of higher harmonics usually requires nonlinear amplifiers biased in weak inversion or even cutoff regions [15]–[18]. This results in narrow locking range, since a strong driving signal is needed to generate the harmonic at the desired power level. Therefore, we choose a PP VCO topology in order to implement the second frequency doubling and relax the requirements on the harmonic generator. Harmonic generator has to generate a second harmonic of the input signal (from 40 to 80 GHz) in order to lock the VCO. The signal strength of the generated second harmonic is much larger than fourth harmonic which would be required if the VCO ran at fundamental 160 GHz. The VCO is implemented as a common-collector Colpitts oscillator for the following reasons. The tank circuit is inherently buffered from the output by a small base–collector capacitance. Colpitts topology allows for simple biasing of the bipolar transistors with respect to cross-coupled configuration, and it can be conveniently combined with accumulation-mode MOS varactors available in the IHP technology.

Placement of the harmonic generator, also called an injector, is critical in terms of an ILFQ locking range. From [12], the maximum locking range of the VCO can be found to be

$$\Delta\omega_{\max} = \frac{I_{\text{inj}}}{I_{\text{osc}}}\frac{\omega_0}{2Q} \tag{21}$$

where I_{inj} and I_{osc} are the injected and free-running VCO currents, ω_0 is the free-running VCO frequency, and Q is the LC-tank circuit quality factor. In order to maximize the locking range, the injected signal should be strong with respect to the VCO signal, whereas Q should be as low as possible to maintain the oscillation. Fig. 15 shows two possible configurations, where a signal V_{inj} is injected into the VCO. In Fig. 15(a) (dashed line), the signal is injected through devices that are placed in parallel with the core transistors [20], [21]. Since V_{inj} pulls the current from the collectors, a small portion of the injected signal leaks to the tank circuit, resulting in poor locking range. We can also imagine connecting the injecting transistors directly to the tank circuit [see Fig. 15(a) (dotted line)], but this would have a heavy impact on the tuning range due to parasitic capacitances associated with the injecting devices. Here, we propose to inject the locking signal through a transformer created from the emitter inductors [see Fig. 15(b)].

Fig. 15(c) shows a VCO half circuit used to determine impedance transformation from harmonic generator output. The oscillation frequency of the Colpitts VCO is

$$\omega_0 = \frac{1}{\sqrt{L_b C_{\text{eq}}}} = \frac{1}{\sqrt{L_b \frac{C_1 C_{\text{eff}}}{C_1 + C_{\text{eff}}}}} \tag{22}$$

where L_b is the base inductor, C_1 is the capacitor shunting the intrinsic nonlinear base–emitter capacitance, and C_{eff} is the effective capacitance given by

$$C_{\text{eff}} = \text{Im}(Y_E)/\omega \tag{23}$$

where Y_E denotes an equivalent admittance of the circuit comprising the transformer. Note that Y_E must be capacitive to provide positive loop gain in the VCO. Typically, L_e is large enough so that the resonant frequency of the C_{var}–L_e network lies well below ω_0. According to [22], L_e improves also VCO tuning range, since the parasitic capacitance of the current source is no longer shunted to C_{var}. Taking the transformer into account [see Fig. 15(c)], the effective impedance Z_{eff} seen at the input of L_e can be expressed as

$$Z_{\text{eff}} = j\omega \underbrace{\left(L_e - \frac{k^2 X_e X_e' L_e'}{{Z_L}^2 + {X_e'}^2}\right)}_{L_{\text{eff}}} + \underbrace{\frac{k^2 X_e X_e'}{Z_L + \frac{{X_e'}^2}{Z_L}}}_{R_{\text{eff}}} \tag{24}$$

where k is the coupling factor, X_e and X_e' are the reactances of L_e and L_e', respectively, and Z_L denotes load impedance presented by the harmonic generator circuit. In general, Z_L is a complex value, but in order to simplify the analysis, we assume Z_L to be real, which is a realistic scenario if the imaginary component is compensated by a matching network. According to (24), Z_L can effectively decrease the inductance and change the resonant frequency of the C_{var}–L_{eff} network so it is instructive to investigate Z_L influence on L_{eff}. Next, we assume the coupling factor k to be 0.6, which is high and still achievable in the used technology. High coupling is desired to maximize the signal injected into the VCO tank circuit. Fig. 16 presents effective inductance and Y_E phase for different real load impedances Z_L. The zero crossing of the Y_E phase indicates the resonant frequency of the C_{var}–L_{eff} network. L_e and L_e' values are arbitrary and serve to depict Z_L influence for different L_e/L_e' ratios. The following observations result from the analysis.

1) The lower Z_L, the lower L_{eff}. In the extreme case, $L_{\text{eff}} = (1 - k^2)L_e$ for $Z_L \to 0$.
2) L_{eff} deviation from L_e is smaller for higher L_e/L_e' ratios.

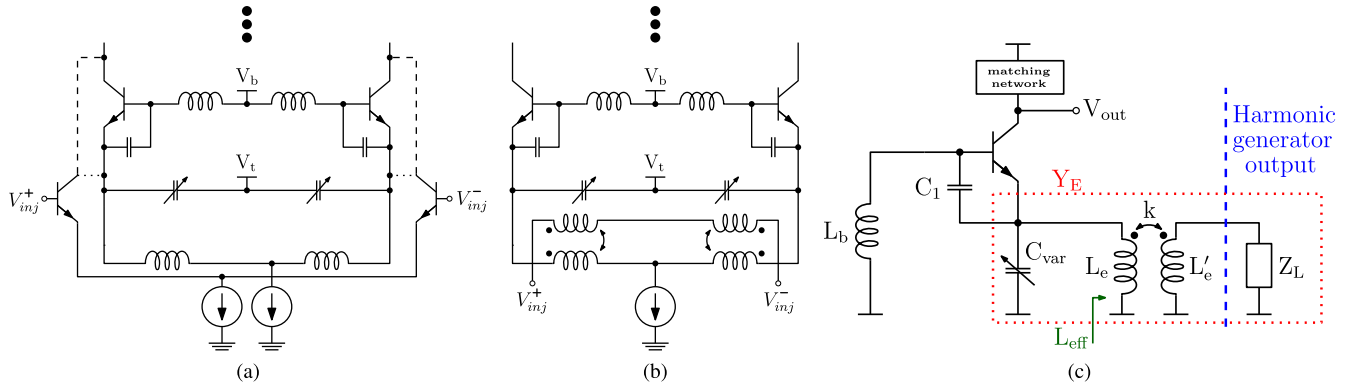


Fig. 15. (a) Conventional direct injection with parallel transistors. (b) Proposed indirect injection using coupled inductors. (c) Half IL-VCO circuit illustrating impedance transformation from the harmonic generator.

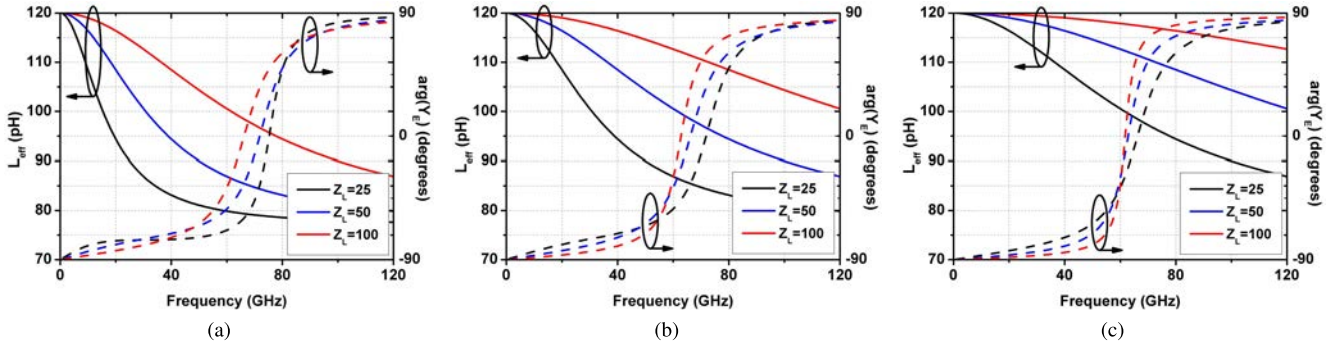


Fig. 16. L_{eff} and Y_E phases for different Z_L values. (a) $L_e = 120$ pH and $L'_e = 240$ pH. (b) $L_e = 120$ pH and $L'_e = 120$ pH. (c) $L_e = 120$ pH and $L'_e = 60$ pH. Phase zero-crossing indicates resonant frequency of the C_{var}–L_e network ($C_{\text{var}} = 50$ fF).

3) High L_{eff} from L_e deviation shifts the resonant frequency of the C_{var}–L_{eff} network toward f_{osc}. As a result, Y_E may not be purely capacitive at f_{osc} and the VCO will fail to oscillate [22].
4) If the transformer is properly designed, i.e., f_0 of the C_{var}–L_{eff} network lies well below VCO frequency range, then the VCO tuning range is only slightly affected, since there are no parasitic components associated with it.

B. Transformer Design

The transformer used to couple the harmonic generator with the PP-VCO was implemented using the topmost thick metal layer TM2 for minimum losses. The L_e/L'_e ratio of around 2 was chosen in order to minimize Z_L influence on L_{eff}. Such ratio [case shown in Fig. 16(c)] ensures that the deviation of L_{eff} from L_e is smaller. This is important since, if L_{eff} decreases too much, the resonant circuit C_{var}–L_{eff} might become inductive. This will cause a Colpitts oscillator not to work, since it needs a capacitive divider created by C_1 and C_{eff}. Here, we chose the primary (L_e) and the secondary coil (L'_e) to have 90 and 41 pH, respectively (Fig. 17). The simulated loss of the transformer is only 1.3–1.4 dB in 70–90 GHz range. A 250 μm-long transmission line TL_e further increases L_{eff} and shifts the resonant frequency of the C_{var}–L_{eff} network down to around 40 GHz. Having a long transmission line is also desired to ease layout implementation of the ILFQ. Minimum spacing (2 μm) between the inductors is applied resulting in a coupling factor of 0.6.

C. Harmonic Generator

Choice of the injector topology is dictated by the efficiency of harmonic signal generation. Since the PP-VCO realizes the second frequency doubling, only the second harmonic of the input signal must be generated by the injector. A bootstrapped GC frequency doubler topology was chosen for its superior conversion gain and differential nature. High CG ensures high input sensitivity and injection efficiency, since low power input signals can lock the VCO. It also helps to increase ILFQ locking range as for a certain input power level, more energy is injected into the VCO. The injected signal strength is limited only by power driving capabilities of the harmonic generator. Two-finger HBTs should provide enough maximum power [see Fig. 4(a)] to lock the VCO.

D. T-ILFQ Implementation

The design flow of the T-ILFQ begins by implementing a PP-VCO, which should be tunable in the desired frequency range. The process of designing a Colpitts VCO is well described in [22]. Then, the emitter inductors must be replaced by a transformer in such a way that the conditions presented in Section III-A are satisfied. This requires a proper transformation ratio L_e/L'_e and load Z_L presented by the harmonic

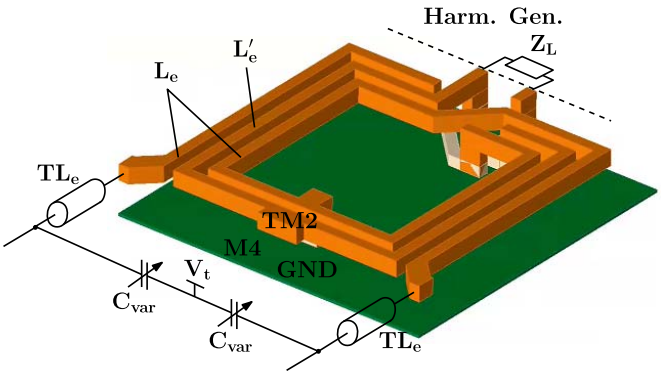


Fig. 17. Layout of the transformer. The loss is 1.3–1.4 dB in 70–90 GHz range.

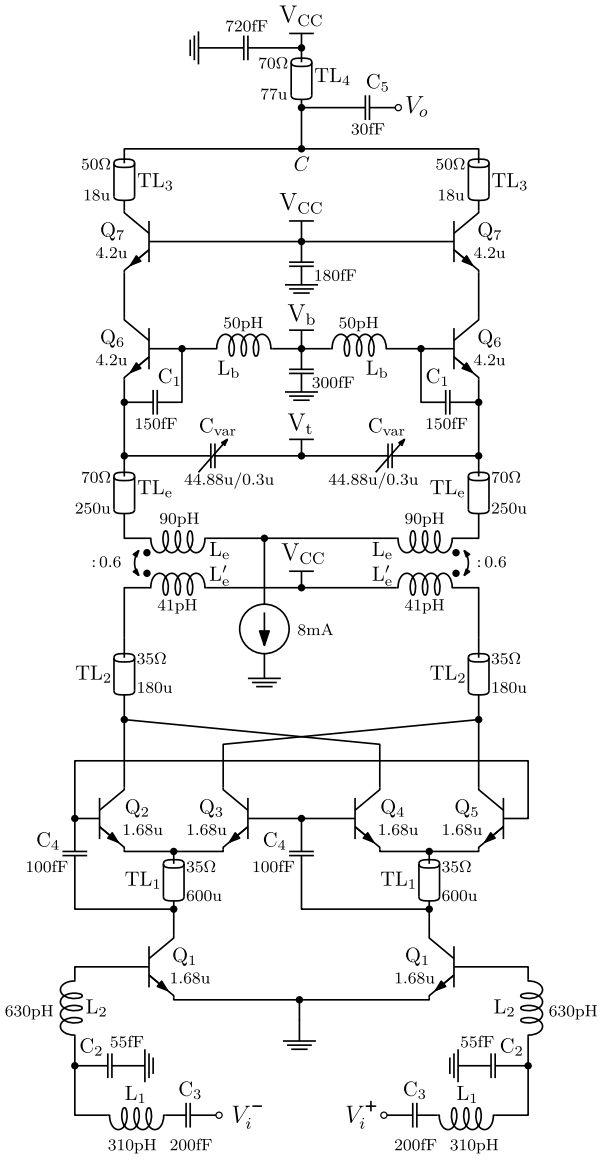
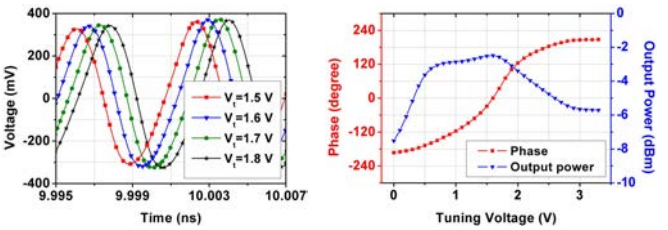


Fig. 18. Schematic of the injection-locked PP FQ.

generator. At the end, the harmonic generator is implemented to provide an efficient second harmonic injection to the VCO.

The schematic of the proposed T-ILFQ is presented in Fig. 18. The 80 GHz VCO is implemented as a common-collector Colpitts circuit. Transistor Q_7 serves as a common-base (CB) buffer to increase the output power and improve isolation between the load and the VCO [22]. The even harmonic signals from both half-circuits add in phase at the common node C while the odd harmonics are canceled. TL_4 and C_5 match the load to the optimum impedance for the highest output power at 160 GHz. The transformer used to couple the VCO tank circuit with the injector is composed of L_e and L'_e. A bootstrapped frequency doubler serves as the harmonic generator. Transmission lines TL_2 compensate the capacitance of Q_{2-5}. A matching network comprising L_1, L_2, C_2, and C_3 match the input to 100 Ω at 40 GHz. The simulated maximum locking range for −10 and 0 dBm input power is 149–172 and 144–186 GHz, respectively, where the whole VCO tuning range was exploited. Fig. 19 shows the simulated waveforms of a locked ILFQ at 160 GHz. By changing the control voltage, the signal phase can be tuned in 0°–360° range showing potential, e.g., for phased-array systems [23].



(a) (b)

Fig. 19. (a) Simulated ILFQ output voltage waveforms at 160 GHz for different tuning voltages. (b) Simulated output power and phase versus tuning voltage at 160 GHz.

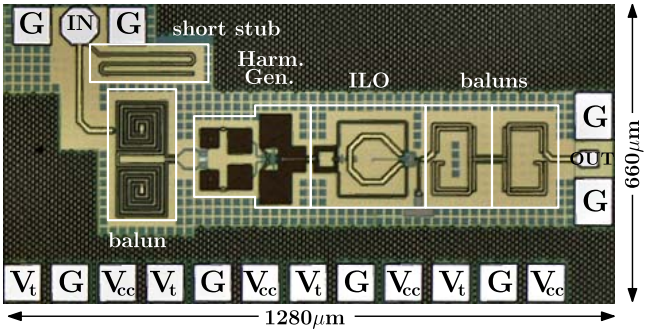


Fig. 20. Chip micrograph.

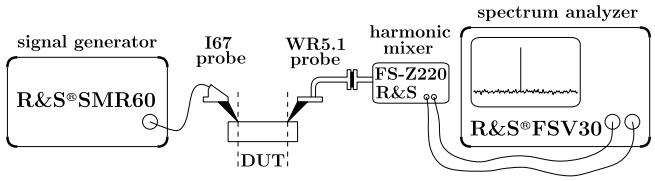


Fig. 21. Setup for the output power and phase noise measurement.

E. Measurement Results

A T-ILFQ was manufactured in a SiGe 130 nm BiCMOS technology using a SG13G2 process of IHP [11]. The die micrograph is shown in Fig. 20. The circuit occupies

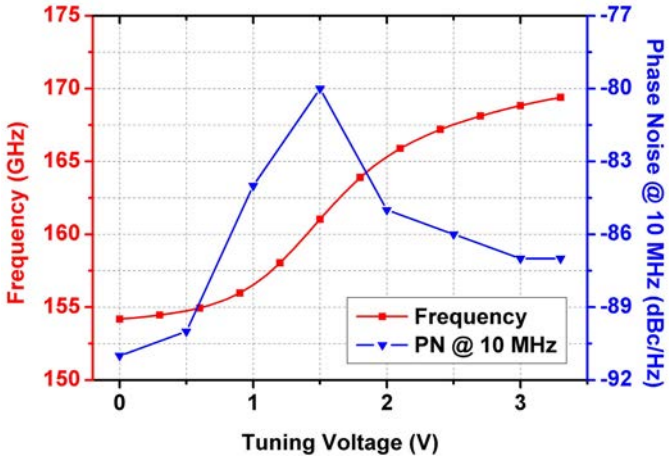


Fig. 22. Measured tuning range and phase noise of the free-running 160-GHz PP-VCO.

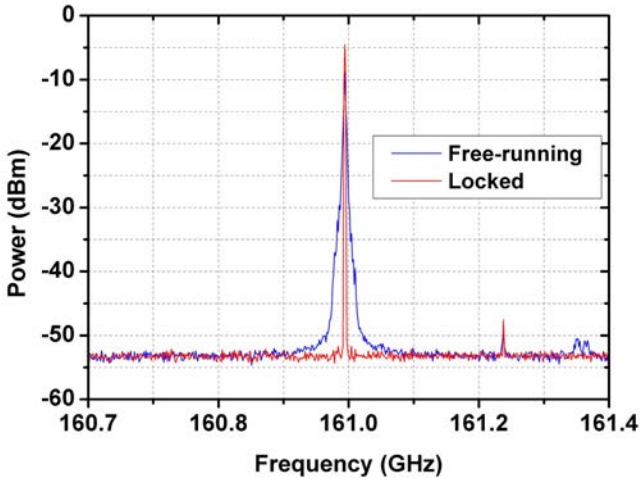


Fig. 24. Spectrum of the free-running and IL VCO.

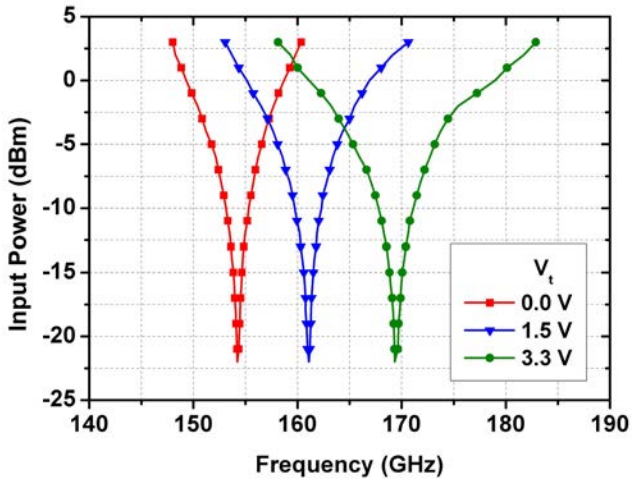


Fig. 23. Measured locking range of the ILFQ.

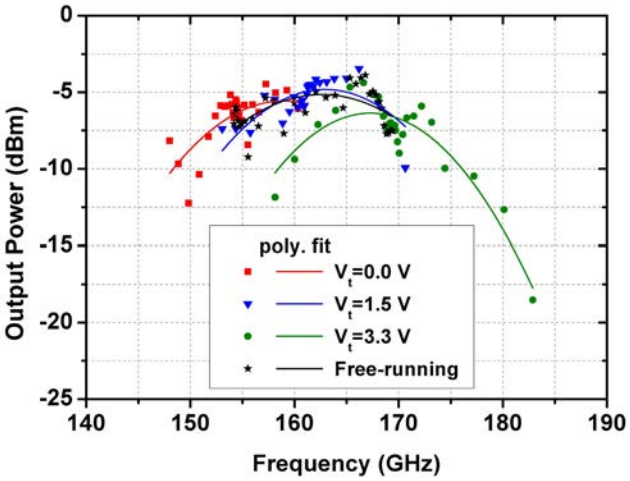


Fig. 25. Measured output power of the ILFQ.

0.84 mm^2, including bondpads and baluns. The size of the ILFQ core is only 0.09 mm^2. First, a free-running 160 GHz PP-VCO was measured in the absence of an injected signal. The setup used to measure the phase noise and output power is presented in Fig. 21. The tuning range as well as the phase noise at 10-MHz frequency offset from the carrier is presented in Fig. 22.

$$L(f_m)[\text{dBc/Hz}] = P_N[\text{dBm}] - P_C[\text{dBm}] - 10\log(\text{RBW[Hz]}) \tag{25}$$

where f_m is the frequency offset, P_N is the noise power at f_m, P_C is the carrier power, and RBW is the bandwidth of an RBW filter in the spectrum analyzer. The VCO can be tuned in 154–169 GHz range, which corresponds to 9.3% tuning range. This is around 25% less than simulated mostly due to not properly modeled varactor capacitance at higher frequencies. The phase noise of a free-running VCO varies in -91 to -80 dBc/Hz range. The worst phase noise is observed in the middle of the tuning range, where the VCO gain reaches the highest value. Next, a 40 GHz signal was applied in order to lock the VCO. Fig. 23 presents measured T-ILFQ locking range for different tuning voltages. As expected, if the quadrupled frequency of V_{inj} is very close to the natural frequency of a free-running VCO, only -22 dBm input signal is needed to lock the VCO. As the input frequency changes, more input power is required in order to lock the VCO. By adjusting V_t, the locking range of the T-ILFQ can be extended and it reaches 35 GHz around 165.5 GHz for $+3$ dBm input power. The ILFQ consumes 14.8 mA from 3.3 V supply. A spectrum of a free-running and locked VCO is shown in Fig. 24 indicating a stable 161 GHz output signal locked to the 40.25 GHz signal coming from the signal generator. Fig. 25 presents measured locked T-ILFQ output power for different tuning voltages and also when the VCO is free-running. For this measurement, a setup presented in Fig. 21 was used. Unfortunately, due to aging and extensive use of the subharmonic mixer, the calibration table no longer fits to reality causing a heavy ripple seen in the measured output power. The T-ILFQ achieves -4 dBm output power at 163 GHz and more than -7 dBm in 153–172 GHz range.

TABLE I
SUMMARY OF STACKED FQ PERFORMANCE AND COMPARISON WITH THE STATE OF THE ART

Ref.	Process	f_T/f_{MAX}	Type	Frequency [GHz]	BW_f^a [%]	P_{sat} [dBm]	CG_{max} [dB]	η_{max}^b [%]	PAE_{max}^c [%]	P_{DC}^d [mW]	Area [mm^2]
[24]	32 nm CMOS	300/350	×4	124-158	24.1	2.3	-21	5.3	<0	32	0.06[e]
[25]	250 nm InP	350/650	×4	110-130	16.6	7	2	10	3.9	47	0.13[e]
[26]	130 nm SiGe	NR	×4	121-137	12.4	-2.4	0.6	1.6	0.2	35	0.03[e]
[27]	130 nm SiGe	NR	×4	124-132.5	6.6	4.4	3	2.4	1.2	115	0.12[e]
[28]	55 nm SiGe	320/370	×4	130-154	16.9	10	5	1.6	1.1	610	0.71[e]
[29]	130 nm SiGe	250/370	×4	128-156	19.7	4	26	1.9	1.9	132	0.11[e]
[30]	90 nm SiGe	300/350	×4	214-245	13.5	2	-10	0.8	<0	200	1.44
[31]	130 nm SiGe	300/500	×2	138-170	20.7	5.6	4.9	10.9	7.6	36	0.48
[32]	250 nm InP	350/600	×2	120-158	27.3	4.2	-2	11.9	<0	19.2	0.18
[32]	250 nm InP	350/600	×3	162-189	15.3	3.8	-1	7.7	<0	26	0.36
This Work	**130 nm SiGe**	**300/500**	×4	**129-171**	**28.0**	**2.2**	**5**	**1.7**	**0.9**	**100**	**0.08**

[a] $BW_f = (f_{max} - f_{min})/f_{center}$, [b] $\eta = P_{sat}/P_{DC}$, [c] $PAE = (P_{out} - P_{in})/P_{DC}$, [d] at P_{sat}, [e] estimated from the chip photo

TABLE II
SUMMARY OF ILFQ PERFORMANCE AND COMPARISON WITH OTHER IL FREQUENCY MULTIPLIERS

Ref.	Process	f_T/f_{MAX}	Type	Frequency [GHz]	Locking Range[a] [%]	P_{out} [dBm]	PAE_{max}^b [%]	P_{DC} [mW]	Area [mm^2]
[15]	65 nm CMOS	NR	×3	85-95.2	5.7	-3.8	8.0	5.2	0.09
[16]	90 nm CMOS	155/250	×3	56-65	14.9	-24.7	<0.1	23.8	0.09
[17]	90 nm CMOS	NR	×3	88.1-108.5	20.7	-15	<0.1	55.2	0.35
[18]	90 nm CMOS	NR	×3	91.2-97.1	6.3	-20	1.0	1	0.49
[33]	65 nm CMOS	185/255	×9	88-99.5	12.3	8.5	1.6	438	0.45
This Work	**130 nm SiGe**	**300/500**	×4	**148-183**	**21.1**	**-4**	**0.8**	**49**	**0.09**

[a] $(f_{max} - f_{min})/f_{center}$, [b] $PAE = (P_{out} - P_{in})/P_{DC}$

IV. CONCLUSION

The performance of the stacked and injection-locked FQs is summarized in Tables I and II, respectively. Due to bootstrapping technique, the stacked FQ achieves the widest bandwidth among other reported circuits providing moderate conversion gain and output power. Since it is a single-branch circuit, the silicon area can be greatly reduced. It is possible to save even more area by replacing long transmission lines with compact inductors. Combination of a Colpitts PP-VCO and bootstrapped frequency doubler enabled the ILFQ to achieve the widest locking range among other IL frequency multipliers while providing moderate efficiency and output power.

To conclude, the stacked FQ is superior in terms of several parameters with respect to injection-locked FQ. It provides wider bandwidth and more output power at the similar DC-to-RF efficiency. However, in a narrower frequency range, the ILFQ can be locked at very low input power levels resulting in high conversion gain. In addition, due to phase shifting potential, it can be used in efficient high frequency phased-array systems. To provide such functionality, the stacked FQ would need to implement additional circuitry resulting in more area and power hungry design. Both FQs show similar performance in terms of power consumption and silicon area.

ACKNOWLEDGMENT

The authors would like to thank J. Borngraeber and C. Wipf for the support during on-wafer measurements.

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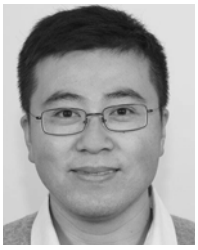

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