A New True-Single-Phase-Clocked Double-Edge-Triggered Flip-Flop for Low-Power VLSI Designs*

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Abstract--- A new CMOS double-edge-triggered flip-flop (DETFF) utilizing true single phase clocking is proposed as a promising storage element in low-power VLSI designs. Compared to the previously reported DETFF's, both the total transistor count and the number of clocked transistors per flip-flop are reduced to save the power consumption.

A clock system is defined in this paper to include a clock generator, clock distribution networks, and clocked flip-flops. Different amounts of power consumption of the different clocking system with different edge-triggered flip-flops are analyzed and compared. It is found that this newly proposed DETFF requires less power in every respect. For example, using the proposed DETFF can save up to 36% of power consumption in the clocking system for a pipelined FIR macro.

I. Introduction

All synchronous digital VLSI systems use one or more clock signals and some kinds of storage elements to form the clocking system to control the data movement. Among all the commonly used storage elements, the timing behaviors of edge-triggered flip-flops (ETFF's) are the simplest [1]. Thus, it is most convenient and straitforward to use edge-triggered flip-flops in the VLSI design, especially in the application-specific IC (ASIC) design. In a well-designed digital VLSI system, the main power consumption will be the part of dynamic power, which is proportional to the clock frequency [2]. Then, it seems natural to use double-edge-triggered flip-flops (DETFF's) in the VLSI design to maintain the same data rate at half the clocking frequency in order to reduce the power consumption of the flip-flop itself [3,4].

True-single-phase clocking (TSPC) [5] has been demonstrated to be an efficient methodology to achieve very high-speed VLSI design. TSPC is also safer and takes less clock signal routing area. A double-edge-triggered flip-flop based on the TSPC technique will be proposed in this paper. Both the total transistor count and the number of clocked transistors per flip-flop are lower than those in previously published DETFF's. Respective power consumptions of the clock generator, global wiring, local wiring, and the flip-flop's are compared for various clocking systems with different flip-flops. The results of HSPICE simulation based on the Kang's method [6] for a pipelined macro [7] show the power consumption of the entire clocking system using the proposed DETFF can save up to 36% compared to that using a TSPC single-edge-triggered flip-flop (SETFF).

II. Power Consumption of a Clocking System

A clocking system [7] is re-defined here so that it includes a clock generator, global wiring, local wiring, and flip-flops (F/F's), as is shown in Fig.1. If the power consumptions of the clock generator, global wiring capacitances, local wiring capacitances, total clocked

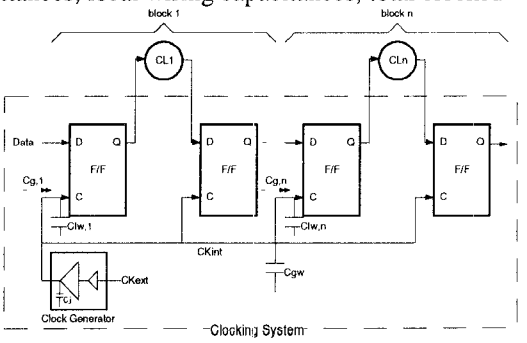

Fig1. The block diagram of a digital VLSI showing the clocking system.

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gate capacitances, and all flip-flops are represented as P_{cg}, P_{gw}, P_{lw}, P_g, and P_{reg}, respectively, the power consumption of the entire clocking system P_{ck} can be expressed as

$$P_{ck} = P_{cg} + P_{gw} + P_{lw} + P_g + P_{reg},$$

$$= \left(1 + \frac{1}{\beta} + \frac{1}{\beta^2} + \cdots + \frac{1}{\beta^N}\right) \cdot V_s^2 \cdot f \cdot \left[C_j + C_{gw} + C_{lw} + C_g\right] + P_{reg}. \quad (1)$$

where

β : tapering factor of the clock generator (clock buffer),

N : number of tapering stages

V_s : voltage swing of the clock distribution network,

f : clock frequency,

C_{gw} : total parasitic capacitance of global wire,

C_{lw} : total parasitic capacitance of local wires,

C_g : total gate capacitance of clocked transistors of the clocking system, and

Cj : junction capacitance of the source-drain regions of the output node of the clock generator.

For the purpose of low power operation, β should be chosen as large as possible [2]. If β=10 is chosen, then eq.(1) can be simplified as

$$P_{ck} \cong 1.11 \cdot V_s^2 \cdot f \cdot \left[C_j + C_{gw} + C_{lw} + C_g\right] + P_{reg},$$

$$= 1.11 \cdot V_s^2 \cdot f \cdot \left[C_j + C_{gw} + C_{lw} + m \cdot C_{gf}\right] + m \cdot P_{gf}, \quad (2)$$

where

m : total number of flip-flops of the clocking system,

C_{gf} : total gate capacitance of clocked transistors per flip-flop, and

P_{gf} : Power consumption of one flip-flop @ frequency f.

From eq.(2), we know that if C_{gw}, C_{lw}, C_{gf}, P_{gf}, and f can be reduced simultaneously, the total power consumption of the whole clocking system may be reduced significantly. C_{gw} and C_{lw} can be reduced if the TSPC scheme can be adopted. C_{gf} can be reduced if the number of clocked transistors can be cut down. P_{gf} can be reduced through novel circuit design, utilization of minimum transistor size, and careful layout design of the flip-flop. Finally, f can be reduced one half if the double-edge-triggered flip-flops can be used instead of single-edge-triggered flip-flops (SETFF's). In the next section, a new TSPC DETFF will be proposed in the hope of fulfilling all the above requirements.

III. TSPC Double-edge-triggered Flip-Flops

Fig.2 shows one positive-edge-triggered flip-flop (PETFF) [5] and three double-edge-triggered flip-flops (DETFF's) [3,4], previously published. If the clock signal cb is generated inside the flip-flop, all the DETFF's of Fig.2 can be considered to be single-phase-clocked.

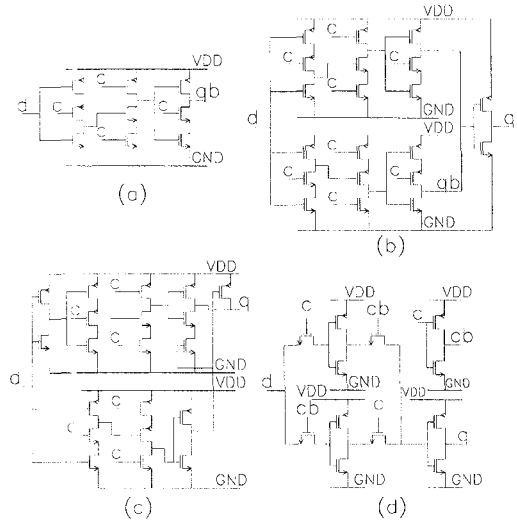

Fig. 2 Conventional edge-triggered flip-flops, (a)PETFF, (b)~(d)DETFF's.

The proposed TSPC DETFF is shown in Fig.3. From the analysis of circuit structure, some characteristics of above flip-flops are listed in Table 1. Normalized P_{cg}, P_w ($P_w = P_{gw} + P_{lw}$), and P_g of each DETFF are also compared, but the influence of P_{reg} has not been considered.

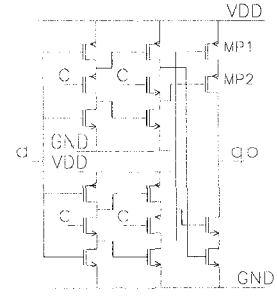

Fig.3 Proposed double-edge-triggered flip-flop.

From Table 1, one may tend to conclude that DETFF's of Fig.2(d) and Fig.3 have the best power

consumption performance mainly because that they have less number of clocked transistors. The influence of P_{reg} will be described in the next section.

Table 1. Features of different edge-triggered flip-flops.

F/F's	s/d	f	Nt	Nc	$P_{cg.n}$	$P_{w.n}$	$P_{g.n}$
Fig.2(a)	s	1	9/11	4	>1	>1	>1
Fig.2(b)	d	1/2	18/20	8	>1	1	>1
Fig.2(c)	d	1/2	20/22	6	>1	1	>1
Fig.2(d)	d	1/2	12/14	4	1	1	1
Fig.3	d	1/2	16/18	4	1	1	1

(1) s/d:s stands for single-edge-triggered, and d for double-edge-triggered. (2) Nt:number of MOS transistors per flip-flop, counting (or without) transistors for generating complementary output signals. (3) Nc:number of MOS transistors clocked by clk per flip-flop. (4)$P_{cg.n}$:normalized P_{cg}. (5)$P_{w.n}$:normalized P_w ($P_w = P_{gw} + P_{lw}$). (6)$P_{g.n}$:normalized P_g.

IV. Speed Figure and Power of ETFF's

In order to study the speed performance of various edge-triggered flip-flops, speed figure τ [7] is defined here as the summation of the setup time $t_{su} = \max(t_{su1} + t_{su2})$ and the clock-to-output delay $t_{cq} = \max(t_{cq1} + t_{cq2})$, as shown in Fig. 4. t_{su1} and t_{cq1} are the setup and clock-to-output times at the rising clock edge, and t_{su2} and t_{cq2} are those times at the falling clock edge. We define the "outputs" to be nodes "qb" in Fig.2(a) and (b) , but nodes "q" in Fig.2(c) and (d). This definition reflects the nature of the minimal function that each flip-flop can accomplish, and the maximum toggle frequency that each flip-flop can achieve. In this paper, t_{su} will be defined as the time interval t_{su} that Data comes before Clock to obtain a minimum summation of t_{su} and t_{cq}.

According to the above definitions, HSPICE circuit simulations based on a 0.6μm single-poly double-metal CMOS technology are made to determine each flip-flop's power consumption and speed figure. To have minimum power dissipation, minimum transistor size (L_{mask}=0.6μm, W_{mask}=1.2μm) is designed for each transistor, and the layout of each transistor is drawn to make the source/drain area as minimized as possible.

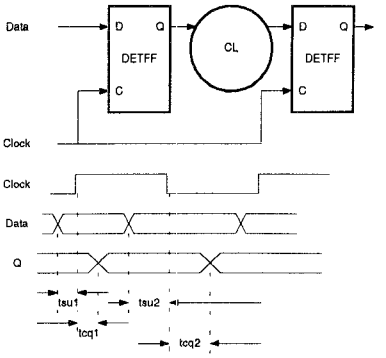

Fig.4 Definition of speed figure

Because the power dissipation depends on the input data pattern, we design a special data pattern as is shown in Fig.5 to simulate these circuits. The pattern corresponds to an input transition probability of 36% with some unfavorable transitions. Simulation results considering the effect of layout are shown in Table 2.

Table 2. Speed/power performance of each edge-triggered flip-flop.

F/F's	t_{cq}	t_{su}	τ	C_{gf}	P_{gf}	C_{ff}(fF)	C_{ff}/C_{gf}
Fig.2(a)	0.36n	0.34n	0.70n	6.88f	P_{2a}:32.46μ	25.97	3.77
Fig.2(b)	0.43n	0.34n	0.77n	13.76f	P_{2b}:26.02μ	41.63	3.03
Fig.2(c)	0.70n	0.30n	1.00n	10.32f	P_{2c}:29.92μ	47.86	4.64
Fig.2(d)	0.53n	0.33n	0.86n	6.88f	P_{2d}:125.4μ	200.6	29.16
Fig.3	0.66n	0.43n	1.09n	6.88f	P_3: 23.38μ	37.41	5.44
Fig.3*	0.58n	0.42n	1.00n	6.88f	P_3*:27.65μ	44.24	6.43

(1)For equal data rate, power consumption is evaluated @25MHz clock rate for double-edge-triggered flip-flops, and evaluated @50MHz clock rate for single-edge-triggered flip-flops..

(2)* : L_{mask}=0.6μm, W_{mask}=2.4μm for M_{p1} and M_{p2}.

From Table 2, we find that the proposed DETFF consumes the least power. The new circuit nonetheless has the largest speed figure due to the path of M_{p1} and M_{p2}. By adjusting the transistor sizes of M_{p1} and M_{p2} a little, the speed figure can be reduced, also shown in Table 2. It is seen that the maximum toggle frequency of the new DETFF can be as high as 500MHz ($= 1/(2 \times speed\,figure)$) after transistor sizing.

V. Total Power Consumption of The Clocking System

Also shown in Table 2 are the two capacitances C_{gf} and C_{ff}. C_{gf} is the clocked gate capacitance per flip-flop.C_{ff} is defined as the equivalent capacitance of one flip-flop, which satisfies

$$P_{gf} = C_{ff} \cdot V_{DD}^2 \cdot f \qquad (3)$$

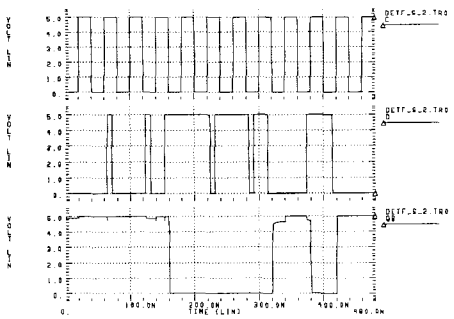

Fig.5 Simulation waveforms of the circuit in Fig.3.

Table 3. A typical power consumption example of different clocking systems(unit of capacitance :pF)

F/F's	f(M)	C_j	C_{gw}	C_{lw}	C_g #	C_{clk}	C_{reg}	C_{tot}	P_{ck} (W)	$P_{ck.n}$ ※	$p \cdot \tau$ ◎
Fig.2a	50	2.3	2.1	11.6	18	37.7	67.9	105.6p	0.132	1.00	35.3
Fig.2b	25	2.3	2.1	11.6	36	57.7	108.9	166.6p	0.104	0.79	30.6
Fig.2c	25	2.3	2.1	11.6	27	47.7	125.2	172.9p	0.108	0.82	41.3
Fig.2d	25	2.3	2.1	11.6	18	37.7	524.9	562.6p	0.352	2.67	115.7
Fig.3	25	2.3	2.1	11.6	18	37.7	97.9	135.6p	0.085	0.64	35.4
Fig.3*	25	2.3	2.1	11.6	18	37.7	115.7	153.4p	0.096	0.73	36.7

:number of flip-flops m = 2616; ※: $P_{ck.n}$:normalized P_{ck};

◎: $p \cdot \tau = (P_{ck} / m) \cdot \tau$ (unit: fJ)

Substituting eq.(3) into eq.(2), we have

$$\begin{aligned} P_{ck} &= 1.11 \cdot V_s^2 \cdot f \cdot \left[C_j + C_{gw} + C_{lw} + m \cdot C_{gf}\right] + m \cdot C_{ff} \cdot V_{DD}^2 \cdot f \\ &= V_s^2 \cdot f \cdot C_{clk} + m \cdot C_{ff} \cdot V_{DD}^2 \cdot f \\ &= V_{DD}^2 \cdot f \cdot \left(C_{clk} + C_{reg}\right), \quad \text{for } V_s = V_{DD} \\ &= V_{DD}^2 \cdot f \cdot C_{tot} \end{aligned} \tag{4}$$

From eq.(4), we can calculate the total power consumption of the whole clocking system for given C_j, C_{gw}, C_{lw}, and m. Taking the pipelined FIR macro in [9] as an example and appling suitable scaling rules, we get a comparison example implemented in a 0.6μm CMOS technology, as is illustrated in Table 3. The scaling factors applied for original C_j, C_{gw}, C_{lw}, and C_g data are 0.46, 0.44, 0.44, and 0.36, respectively. From Table 3, it is seen that the total power consumption of the clock system of the proposed DETFF, compared with the SETFF of Fig.2(a), can save up to 36%. If P_{ck} is devided by m and then multiplied by the speed figure, we have an effective power*delay product index $p \cdot \tau$ for each flip-flop. From Table 3, it is also found that the proposed DETFF has a very challenging power-delay product performance.

VI. Conclusion

A CMOS double-edge-triggered flip-flop (DETFF) with true single phase clocking is proposed. Considering the power consumption in the whole clocking system, it is found that the proposed DETFF can save up to 36% power consumption for a pipelined FIR macro. Meanwhile, by using an advanced 0.6μm CMOS process technology, the proposed DETFF can achieve 1GHz data rate. It is then concluded that the proposed DETFF can be used as a promising storage element in low-power or even high-speed VLSI designs.

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