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A New IIP2 Enhancement Technique for CMOS Down-Converter Mixers

Mohammad B. Vahidfar, *Student Member, IEEE*, and Omid Shoaei, *Member, IEEE*

***Abstract*—The design of a CMOS mixer for cellular phone and 3G applications is challenging because of tough linearity and noise requirements. A new technique for second-order input intercept point (IIP2) enhancement of CMOS down-converter mixers is introduced in this brief. The technique is based on canceling second-order intermodulation components generated in input pseudodifferential transconductor, by injecting a nonlinear current to the mixer. Since this current is controlled by a high bandwidth feedback loop, the cancellation technique can be used in multistandard mixers for high channel bandwidth applications like UMTS and IEEE802.11 as well as GSM. A CMOS mixer demonstrating the performance for UMTS standard is designed in a 65-nm technology which can work with supplies as low as 1 V. The simulation results show that the differential and common mode IIP2 of the mixer are improved about 22 and 29 dB, respectively, while cancellation circuit consumes less than 3.3 mA. The other mixer parameters such as noise figure are not affected by the proposed technique.**

***Index Terms*—CMOS, mixer, second-order intermodulation (IM2).**

I. Introduction

CMOS direct-conversion receivers are generally used in modern wireless terminals because of high integration level, low cost and simplicity of base-band circuitry. However, several challenging issues including second-order intermodulation (IM2) and flicker noise appear in this kind of receivers. The most dominant source of IM2 and flicker noise in a direct-conversion receiver is the down-converter mixer [1]–[4], because most of low-noise amplifier (LNA) contribution is filtered out by its output narrowband *LC* resonator and ac coupling between LNA and mixer.

Generally, a double-balanced Gilbert-cell mixer with active transconductor is used for I and Q down conversion. In a perfectly balanced case, the even-order distortion caused by device nonlinearity would not appear in the signal path. However, in a practical situation where mismatch in the load and switching transistors exist, the even-order intermodulation appears in the signal path. The even-order nonlinearity can be reduced by using differential topology and symmetric layout, but the required performance especially for cellular phone applications can not be met. Therefore, using some second-order input intercept point (IIP2) improvement techniques is necessary.

An effective but expensive solution for improving IIP2 is using an external surface acoustic wave (SAW) filter between LNA and mixer in order to make the mixer linearity requirement relaxed by attenuating the out of bands blockers [5]. Recently, some calibration circuits have been proposed to address IIP2 problem but they are complex and large power consuming [6], [7]. Using analog techniques and optimizing the mixer for IIP2 is the other approach [8], [9]. In this frame work the IIP2 of switching pairs and transconductor which are the main source of IIP2 degradation in an active mixer should be enhanced [8].

Generally, a low-voltage active mixer is made by cascading of pseudodifferential transconductor, switching pairs and load. In gigahertz frequencies flicker noise and IM2 of the switching pairs are minimized by using an *LC* filter which tunes the parasitic capacitor of switching transistors in local oscillator (LO) frequency [8], [10]. However, in a perfectly tuned switching stage, the IIP2 of the mixer is also usually lower than the cellular phone requirement, because of the large common mode IM2 components ($\mathrm{IM2_{CM}}$) generated in the pseudodifferential transconductor. As the following equation of the input intercept second-order voltage point (IIV2) shows, these CM currents ($I_{\mathrm{IM2,CM}}$) are converted to differential products by the LO switching pairs asymmetry and load mismatch and are added to the other differential IM2 currents ($I_{\mathrm{IM2,diff}}$) in the mixer output [11]

$$\mathrm{IIV2}=\frac{2}{\pi}\frac{gm_{\mathrm{RF}}\cdot v_{\mathrm{RF}}^2}{\sqrt{L^2\left(I_{\mathrm{IM2,diff}}^2+I_{\mathrm{IM2,CM}}^2\right)+\left(\frac{\sigma_R}{R_L}\right)^2 I_{\mathrm{IM2,CM}}^2}} \tag{1}$$

in which gm_{RF}, R, σ_R, and L are the input mixer transconductance, output mixer resistance, standard deviation of mismatch in the output load, and low-frequency leakage of the switching transistors, respectively.

This problem is addressed in [8] by a *RC* degenerative input stage. However, it cannot be used with low-voltage supplies, because of using stacked transistors and consuming more than 600 mV in the input stage. This technique is used in [12] for a low-voltage application by using a folded architecture. A low-voltage solution in which a feedback loop is employed for attenuating $\mathrm{IM2_{CM}}$ is presented in [9] for GSM receivers. However, it is not applicable for high bandwidth applications like UMTS, because the bandwidth of the feedback loop is low. This bandwidth is dominated by several poles such as the two poles of the compensated amplifier and the current injecting transistor and the pole generated by the CM part of the mixer load [9]. To meet the required IIP2 performance by using this approach, the gain bandwidth product (GBW) of the feedback loop which is 10 MHz in GSM should be greater than 200 and 250 MHz for UMTS and IEEE802.11, respectively.

In this brief, the poor IIP2 performance of the input stage of the mixer is addressed by a new circuit which is based on attenuating $\mathrm{IM2_{CM}}$ products by injecting a nonlinear current

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M. B. Vahidfar is with the Dipartimento di Elettronica, Università degli studi di Pavia, 27100 Pavia, Italy (e-mail: Mohammad.vahidfar@unipv.it).

O. Shoaei is with IC design Lab, ECE Department, University of Tehran, Tehran 14395-515, Iran (e-mail: oshoaei@ut.ac.ir).

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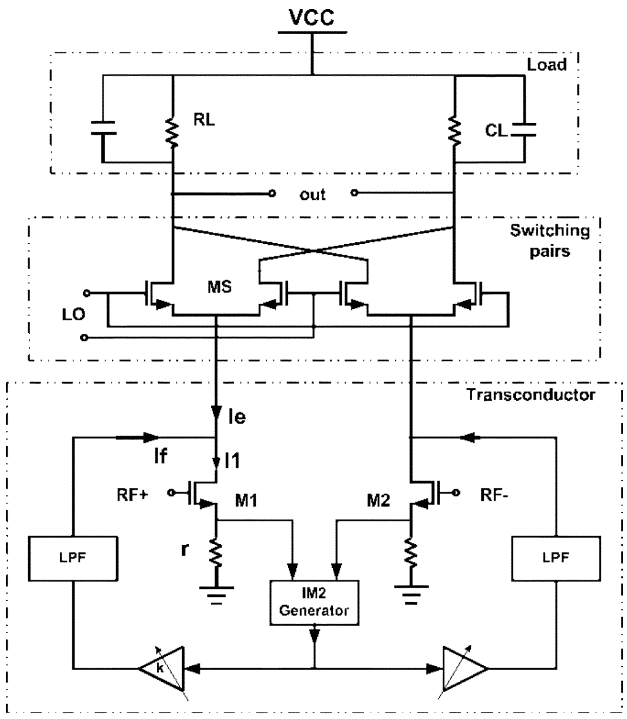

Fig. 1. Block diagram of the IM2 cancellation technique.

into the mixer. The proposed circuit works for both high and low bandwidth receivers and consequently is a good candidate for multistandard mixers. Moreover, the circuit can work with supplies as low as 1 V.

The brief is organized as follows. The IIP2 improvement technique and its circuit implementation are discussed in Section II. The designed mixer is presented in Section III. The simulation results are discussed in Section IV which is followed by conclusion.

II. IIP2 Improvement Technique

A. IM2 Cancellation Mechanism

A simple model of the proposed IM2 cancellation technique is shown in Fig. 1. An IM2 generator block senses the current of the transconductor and regenerates the required $\mathrm{IM2_{CM}}$. For simplicity, suppose this current sensing is done by a small resistor r in the source of input transistors. The generated current is amplified, filtered out and then is injected to the output of M1 and M2 transistors. The amplitude of the injected current should be controlled in order to cancel the $\mathrm{IM2_{CM}}$ current of transconductor.

Referring to Fig. 2, it is supposed that M3 and M4 transistors, connected to the input RF signals, are similar. Since the output of these two transistors are connected together, the differential components of their currents including signal current $\mathrm{IM2_{diff}}$ and other differential intermodulated components do not appear in the sum of their output currents (I_{OL}). This is shown by

$$\begin{aligned} I_{\mathrm{OL}} &= I_3 + I_4 \\ &= I_{\mathrm{IM2,CM,OL}}(\mathrm{M3}) + I_{\mathrm{IM2,CM,OL}}(\mathrm{M4}) + I_{\mathrm{IMy,CM}} \end{aligned} \tag{2}$$

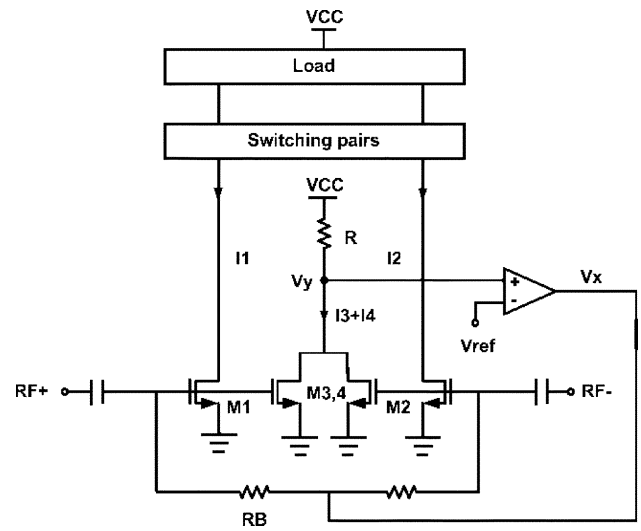

Fig. 2. Mixer enhanced by the IM2 cancellation loop.

where $I_{\mathrm{IM2,CM,OL}}(\mathrm{M3})$ and $I_{\mathrm{IM2,CM,OL}}(\mathrm{M4})$ show the $\mathrm{IM2_{CM}}$ current of transistors M3 and M4, respectively, and $I_{\mathrm{IMy,CM}}$ represents all CM even-order distortions except the second-order one.

The first two terms of the Taylor series expansion of the I–V characteristic of a MOS transistor is expressed as

$$i = gm \cdot v_{gs} + g_2 \cdot v_{gs}^2. \tag{3}$$

By using (2) and (3) and considering the second-order distortion

$$I_{\mathrm{OL}} = 2I_{\mathrm{IM2,CM,OL}}(\mathrm{M3}) = 2g_2 \cdot (v_{\mathrm{in}})^2. \tag{4}$$

in which v_{in} is the RF signal applied to the input RF+ and RF- nodes by different polarity.

Now consider a negative feedback loop around M3 and M4 transistors made by an amplifier and a *RC* filter, as it is shown in Fig. 2. Equation (2) in the closed-loop condition is

$$\begin{aligned} I_{\mathrm{CL}} &= I_3 + I_4 \\ &= I_{\mathrm{IM2,CM,CL}}(\mathrm{M3}) + I_{\mathrm{IM2,CM,CL}}(\mathrm{M4}) + I_{\mathrm{IMz,CM}} \end{aligned} \tag{5}$$

where $I_{\mathrm{IM2,CM,CL}}(\mathrm{M3})$ [$I_{\mathrm{IM2,CM,CL}}(\mathrm{M4})$] shows the $\mathrm{IM2_{CM}}$ current of M3 (M4) transistor in closed-loop condition.

By considering (3) and (5)

$$I_{\mathrm{CL}} = gm_3 \cdot v_{gs,\mathrm{M3}} + gm_4 \cdot v_{gs,\mathrm{M4}} + g_2 \cdot (v_{gs,\mathrm{M3}} + v_{gs,\mathrm{M4}})^2 \tag{6}$$

where gm_3 and gm_4 are the transconductance of transistors M3 and M4, respectively. The v_{gs} of transistors M3 and M4 is calculated by the small-signal analysis of the loop

$$\begin{cases} v_{gs,\mathrm{M3}}(s) = \frac{1}{1+R_B \cdot C \cdot s}(R_B \cdot C \cdot s \cdot v_{\mathrm{in}} + v_x) \\ v_{gs,\mathrm{M4}}(s) = \frac{1}{1+R_B \cdot C \cdot s}(-R_B \cdot C \cdot s \cdot v_{\mathrm{in}} + v_x). \end{cases} \tag{7}$$

in which v_x is the voltage at the output of amplifier.

Using (4)–(7) and assuming that 3-dB frequency of *RC* filter is higher than IM2 components frequency and also is one decade lower than RF frequencies, the following relationship between

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$\mathrm{IM2_{CM}}$ current of transistor M3 (M4) in open- and closed-loop conditions is derived

$$I_{\mathrm{IM2,CM,CL}}(\mathrm{M3}) = I_{\mathrm{IM2,CM,OL}}(\mathrm{M3}) + gm_3 \cdot v_x. \quad (8)$$

Moreover, referring to (5) and Fig. 2 and neglecting CM intermodulated components with order higher than 2, the following equation is obtained :

$$I_{\mathrm{IM2,CM,CL}}(\mathrm{M3}) + I_{\mathrm{IM2,CM,CL}}(\mathrm{M4}) = -\frac{v_x}{A \cdot R} \quad (9)$$

where A is the gain of amplifier.

From (8) and (9), it can be concluded that

$$I_{\mathrm{IM2,CM,CL}}(\mathrm{M3}) = \frac{I_{\mathrm{IM2,CM,OL}}(\mathrm{M3})}{1 + A \cdot (gm_3 + gm_4) \cdot R}. \quad (10)$$

The above equation shows that the $\mathrm{IM2_{CM}}$ current of M3 transistor is attenuated in the feedback loop by the loop gain (LG) as it was expected from the feedback theory. Also the LG is

$$\mathrm{LG} = A \cdot (gm_3 + gm_4) \cdot R = 2A \cdot gm_3 \cdot R. \quad (11)$$

Equation (9) can be simplified as below

$$v_x = (-2A \cdot R)\, I_{\mathrm{IM2,CM,CL}}(\mathrm{M3}). \quad (12)$$

Moreover; using (10) and (12) and assuming high-loop-gain condition (LG $\gg$ 1)

$$v_x \approx -\frac{I_{\mathrm{IM2,CM,OL}}(\mathrm{M3})}{gm_3}. \quad (13)$$

In the other words, this voltage which is made by the feedback loop is responsible for attenuating the $\mathrm{IM2_{CM}}$ current in M3 and M4 transistors.

Considering that M1 and M3 transistors are in parallel and also v_x acts as a common mode voltage for all M1, M2, M3 and M4 transistors then

$$I_{\mathrm{IM2,CM,CL}}(M1) = I_{\mathrm{IM2,CM,OL}}(M1) + gm_1 \cdot v_x \quad (14)$$

where $I_{\mathrm{IM2,CM,CL}}(M1)$ and $I_{\mathrm{IM2,CM,OL}}(M1)$ are the $\mathrm{IM2_{CM}}$ current of M1 transistor when the mixer is with and without the feedback loop, respectively.

Considering (13) and (14) then

$$\frac{I_{\mathrm{IM2,CM,CL}}(M1)}{I_{\mathrm{IM2,CM,OL}}(M1)} = 1 - \frac{gm_1}{gm_3} \cdot \frac{I_{\mathrm{IM2,CM,OL}}(\mathrm{M3})}{I_{\mathrm{IM2,CM,OL}}(M1)}. \quad (15)$$

As it is shown in [11], the $\mathrm{IM2_{CM}}$ of pseudodifferential is proportional to g_2 which, as explained in (3), is the second-order coefficient of the MOS I–V characteristic

$$I_{\mathrm{IM2,CM}} \propto g_2. \quad (16)$$

Therefore, considering (15) and (16)

$$\frac{I_{\mathrm{IM2,CM,CL}}(M1)}{I_{\mathrm{IM2,CM,OL}}(M1)} = 1 - \frac{gm_1}{gm_3} \cdot \frac{g_{2,\mathrm{M3}}}{g_{2,M1}}. \quad (17)$$

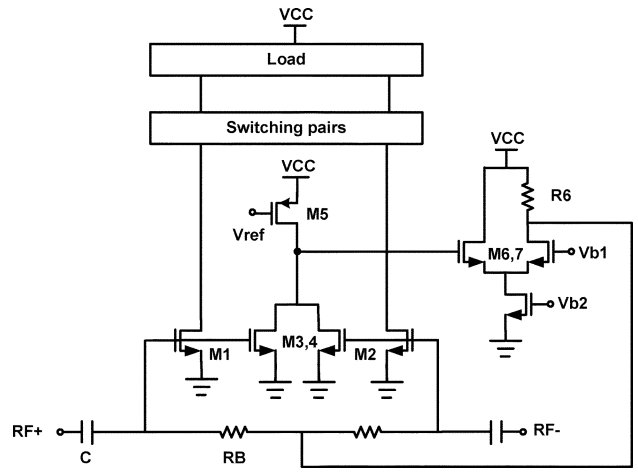

Fig. 3. Circuit implementation of the IM2 cancellation technique.

From this equation, it is concluded that $\mathrm{IM2_{CM}}$ current of M1 transistor can be canceled if the following equation is satisfied :

$$\frac{gm_3}{g_{2,\mathrm{M3}}} = \frac{gm_1}{g_{2,M1}}. \quad (18)$$

For the CMOS transistors in the strong inversion region the g_2 is

$$\frac{g_2}{gm} = \frac{gm}{I} \frac{2}{(1 + \theta v_{\mathrm{od}})^2} \approx \frac{2}{v_{\mathrm{od}}(1 + \theta v_{\mathrm{od}})^2} \quad (19)$$

where v_{od} and θ are overdrive voltage and fitting parameter for mobility, respectively [13].

Therefore; it can be concluded that the above condition ((18)) can be satisfied by proper sizing and biasing of transistor M3.

In conclusion, the $\mathrm{IM2_{CM}}$ components generated in M1 and M2 transistors are canceled by employing a feedback loop which attenuates the $\mathrm{IM2_{CM}}$ current of M3 and M4 transistors. However referring to (17)–(19), the mismatch between M1 and M3 transistors degrades this IM2 cancellation.

B. Circuit Implementation

Fig. 3 shows the implementation of the proposed IM2 cancellation technique. The required LG is provided by two stages of the gain. The first one is made by M5, M3 and M4 transistors and the second one is implemented by a differential common gate (M6 and M7 transistors). To ensure the loop stability, the loop is compensated by a LPF made by R_B and C. The second pole of the loop is in the output of M5 transistor which is very far from the first pole because of low capacitance load of this node. Moreover the bias current of M3 and M4 are chosen high enough to ensure high bandwidth in this node. The bias current of M5 transistor is set to 1.8 mA and consequently that of M3 transistor is 0.9 mA.

The loop gain in dc is 41 dB, while the unity gain frequency and phase margin of the loop are 250 MHz and 70 deg, respectively. The IM2 cancellation circuit bandwidth should be higher than half of the signal bandwidth in a zero intermediate frequency (IF) receiver. Therefore, the proposed circuit can work for high channel bandwidth applications like UMTS with 4-MHz channel bandwidth as well as GSM with 200 kHz.

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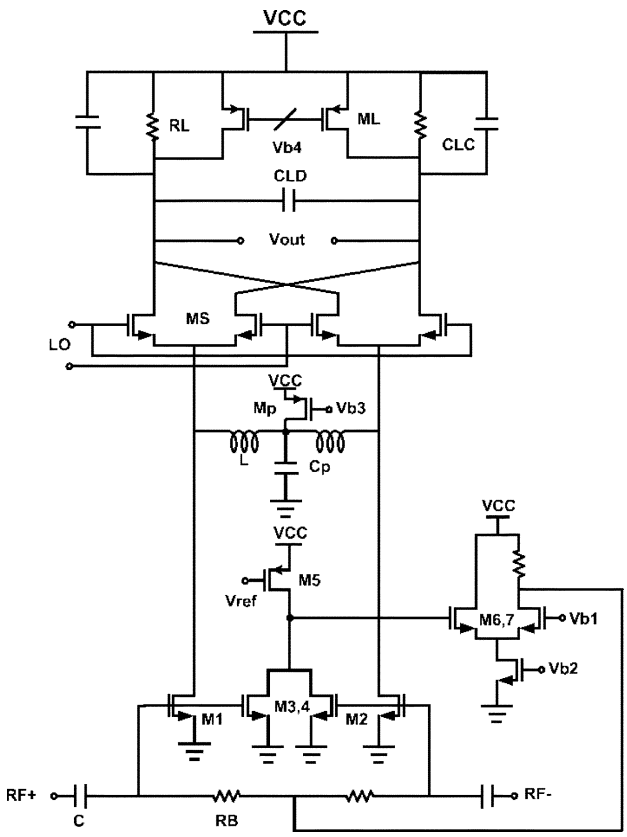

Fig. 4. Proposed mixer.

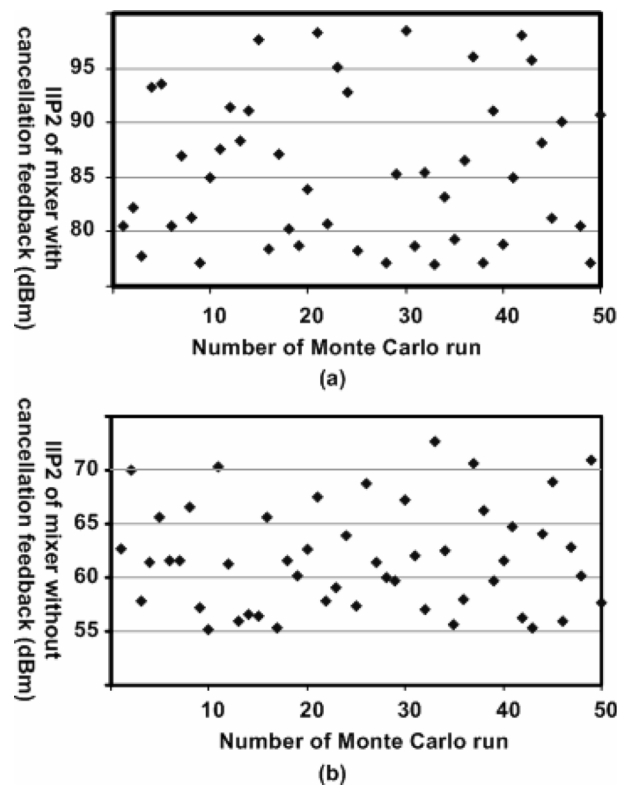

Fig. 5. (a) Result of Monte Carlo analysis of the enhanced mixer. (b) Result of Monte Carlo analysis of the conventional mixer.

The proposed IM2 cancellation circuit does not affect the mixer noise figure (NF) because both thermal and flicker noises, generated in the circuit, are injected to the mixer as a common mode noise and consequently are rejected in the mixer output.

The minimum supply voltage of the proposed circuit is equal to $V_{\mathrm{TH}} + 3V_{\mathrm{od}}$, in which V_{TH} is the threshold voltage of nMOS Transistors. This minimum voltage is less than 1 V if V_{TH} is less than 500 mV and V_{od} is considered 150 mV.

III. Proposed Mixer

A mixer, enhanced by the proposed cancellation technique, for UMTS application is designed, in order to demonstrate the performance of the technique (Fig. 4).

The $\mathrm{M1}$ and $\mathrm{M2}$ transistors, sized by 120 μm/0.15 μm, are biased by 4.5 mA, which 1.5 mA of this bias current is sourced by M_p and the rest comes from the switching pairs. In this way, there is a degree of freedom for choosing the transconductor bias current for the optimized IIP3 performance, independent of the bias current of the switching pairs which highly affects the mixer NF.

The switching transistors (M_s), sized as 400 μm/0.24 μm in order to achieve the optimum flicker noise and IIP2 performance, are derived by a local oscillator with 5-dBm power. To maximize the mixer dynamic range the parasitic capacitor of the switching transistors is tuned in the LO frequency by a *LC* filter [8], [9]. The quality factor of the differential inductor (Q) is about 10 in the working frequency. This inductor is grounded by a large capacitor C_P (25 pF) in RF frequencies. Additionally, the differential part of IM2 generated in the mixer input transistors is also re-circulated by the inductor by making the output of $\mathrm{M1}$ and $\mathrm{M2}$ transistors shorted in IF frequencies.

Two pMOS transistors (M_L) with long channels are responsible for providing biasing current in the mixer output. Two *RL* resistors providing required conversion gain are also shunted with M_L transistors for reduction of their current and achieving lower voltage headroom. The common- and differential-mode filtering in IF is done by CLC and CLD capacitors.

IV. Simulation Results

The design was done in a 65-nm CMOS technology. The IIP2 simulation is done in the worst case condition by applying offset voltages equal to 3 times of the standard deviation mismatch (σ) to all transistors [8], [11]. These mismatches are calculated based on the process information and are verified by Monte Carlo simulations.

The IIP2 simulation is done by two-tone test at 1.98 GHz with different spacing less than 10 MHz which emulates the TX leakage as the main blocker while the LO frequency is 2.11 GHz. The Monte Carlo simulation of the mixer with and without cancellation loop is depicted in Fig. 5. It shows that the IIP2 of the mixer enhanced by the cancellation feedback is higher than 75 dBm which is required in cellular phones [6], while in the conventional mixer it is between 55 and 73 dBm. Moreover it shows that the mixer achieves about 22-dB improvement in IIP2 in the expense of about 40% current consumption increase.

Fig. 6 shows the $\mathrm{IIP2}_{\mathrm{CM}}$ of the mixer with and without cancellation feedback which is compared with $\mathrm{IIP2}_{\mathrm{CM}}$ of the IM2

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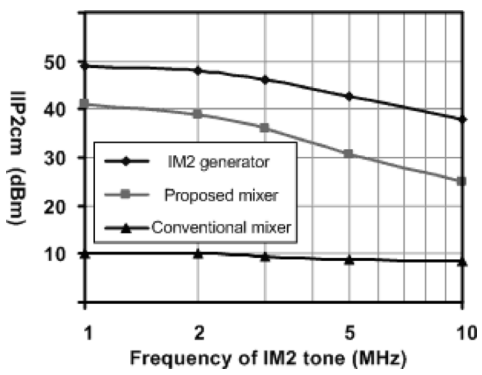

Fig. 6. The $\mathrm{IIP2}_{\mathrm{CM}}$ of the mixer with and without cancellation loop versus the frequency of the IM2 tone besides the $\mathrm{IIP2}_{\mathrm{CM}}$ of IM2 generator.

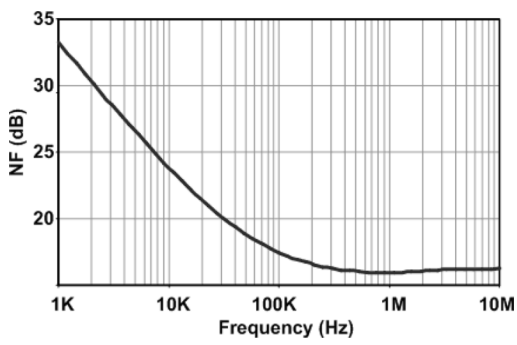

Fig. 7. The NF of the designed mixer.

generator. It can be concluded that the mixer achieves about 31-, 29-, and 17-dB improvement in $\mathrm{IIP2}_{\mathrm{CM}}$ in GSM, UMTS and IEEE802.11, respectively. The improvement of $\mathrm{IIP2}_{\mathrm{CM}}$ in IEEE802.11 is lower than UMTS because of the lower LG of the cancellation loop in 10 MHz comparing to 2 MHz. However, the IIP2 requirement of IEEE802.11 can also be met because it is more relaxed than that of cell-phone mixers [12]. Moreover this figure shows that the attenuation of $\mathrm{IM2}_{\mathrm{CM}}$ current of $\mathrm{M1}$ transistor (Fig. 4) is less than that of $\mathrm{M3}$ transistor (IM2 generator), because the IM2 cancellation performance in $\mathrm{M1}$ transistor is degraded by mismatch between $\mathrm{M1}$ and $\mathrm{M3}$ transistors.

The input referred noise, which is in-band averaged noise (10 kHz–1.92 MHz), is less than 3.4 nV/sqrt(Hz). The mixer NF performance is shown in Fig. 7.

The third-order nonlinearity is simulated with the transmitter signal leakage intermodulating with a blocker which is 67.5 MHz away from the receive band. The mixer IIP3, conversion gain and power consumption are 8 and 12 dBm and 8.5 mW, respectively.

V. Conclusion

A new cancellation technique for improving mixer IIP2 performance is proposed in this brief. The $\mathrm{IM2}_{\mathrm{CM}}$ generated in the pseudodifferential input stage of the mixer is attenuated by employing a feedback loop. Making use of this feedback loop about 22-dB improvement in the mixer IIP2 is achieved. The mixer meets the tough cellular phone IIP2 requirement while it does not affect other mixer parameters like NF. The design works with low supply voltages and has enough bandwidth for high bandwidth applications like UMTS and IEEE802.11. Therefore, it is a good candidate for high IIP2 multistandard mixers. The linearity and noise performance of this mixer serves the demand of fully integrated, hardware shared universal mobile terminal.

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