A High IIP2 Mixer Enhanced by a New Calibration Technique for Zero-IF Receivers

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***Abstract*—The second-order intercept point (IP2) performance of direct conversion receivers is limited by the second-order nonlinearity of the mixer. A new technique which is based on calibrating mixer by injecting a programmable nonlinear current into the mixer output is introduced in this paper. The proposed calibration technique can be used in multistandard mixers. A CMOS mixer demonstrating the performance for Universal Mobile Telecommunication System application and working with supplies as low as 1 V is designed in a 65-nm technology. The simulation results show that the mixer IIP2 is improved more than 25 dB while the mixer current consumption is increased less than 1 mA. The calibration circuit is low noise not to affect the mixer noise figure.**

***Index Terms*—Calibration, CMOS, mixer, second-order input intercept point (IIP2), second-order intermodulation (IM2).**

I. Introduction

THE DIRECT conversion receivers are very attractive because of high integration level, low cost, and simplicity of baseband circuitry. However, several challenging issues including second-order intermodulation (IM2) appears in this kind of receivers. The most dominant source of IM2 in a direct conversion receiver is the down-conversion mixer [1], [2]. This is because most of the low-noise amplifier (LNA) contribution is filtered out by its output narrowband *LC* resonator and ac-coupling between LNA and mixer.

Conventionally, balanced circuits with differential inputs and outputs and symmetric layout are used to minimize the even-order distortion effects. However any mismatches like nonideal duty cycle of local oscillator (LO) clocks, gain mismatch between the two sides of a differential circuit and mismatch in the load resistance make the differential circuits unbalanced and generate even-order distortion terms. Therefore, to meet the required second-order input intercept point (IIP2) performance, especially for cellular phone applications, using some on-chip calibration circuits [3], [4] or analog techniques [5], [6] is necessary. The analog techniques contrary to the calibration circuits are sensitive to temperature and voltage variations. Moreover, they often compromise other parameters of mixer like voltage headroom [5] or they work only in specific applications [6].

On the other hand, migration to the sub-scaled CMOS technologies forces the circuits to work with low-voltage supplies [7]. Additionally, a strong interest towards solutions work in multistandard mobile terminals has been created by the evolution of wireless communication.

In this paper, a new low-voltage calibration technique for attenuating IM2 components in the multistandard mixer is presented. The performance of this calibration circuit is demonstrated in a high IIP2 mixer supporting Universal Mobile Telecommunication System (UMTS) standard.

The paper is organized as follows. The IIP2 calibration technique and its circuit implementation are discussed in Section II. The designed mixer is presented in Section III. The simulation results are discussed in Section IV which is followed by conclusion.

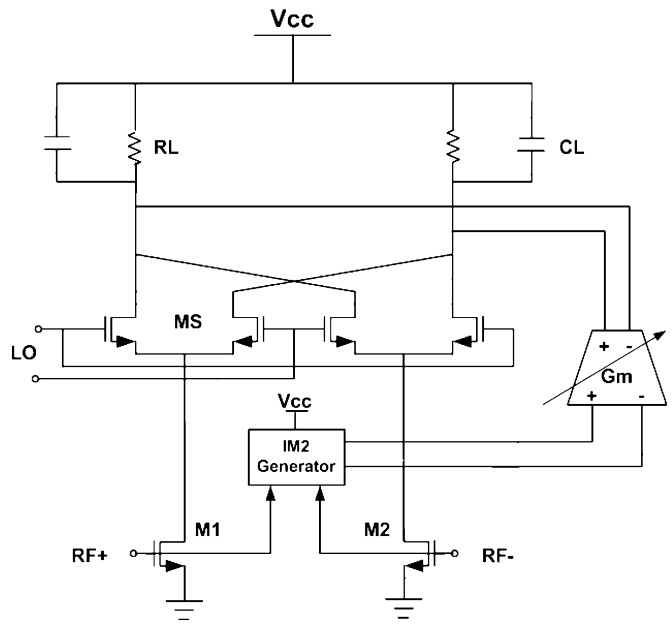

Fig. 1. Block diagram of the IIP2 calibration technique.

II. IIP2 Calibration Technique

A. Second-Order Nonlinearity Sources

Generally, a low-voltage active mixer is made by a stack of pseudodifferential input stage, switching transistors and load (Fig. 1). In gigahertz frequencies the IIP2 performance of the mixer is degraded mainly by the parasitic capacitor of the source node of the switching transistors (C_P).

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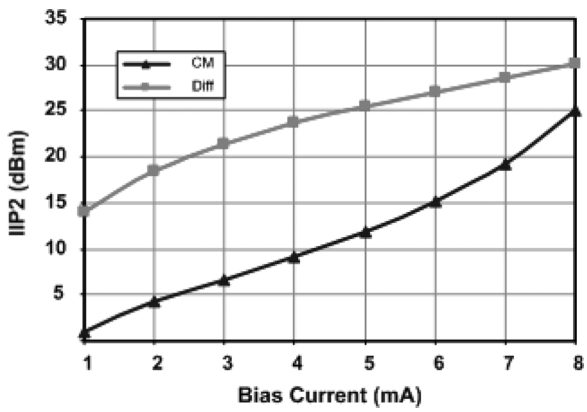

Fig. 2. CM and differential IIP2 of a pseudodifferential transconductor versus biasing current ($W = 120\ \mu$m, $L = 0.15\ \mu$m).

The random mismatch between switching transistors can be modeled by an offset voltage [5], [8]. The parasitic capacitor C_{P} is charged and discharged by this offset voltage in each $\mathrm{F_{LO}}$ period in which $\mathrm{F_{LO}}$ is the frequency of local oscillator (LO). The low pass behavior of the source node of the switching transistor causes a nonlinear current, which is modulated by transconductor intermodulated components, injected to the switching transistors [8]. This IM2 current is appeared at the mixer output after down-converting by the switching transistors.

Moreover, in a perfectly tuned switching stage, the IIP2 of the mixer is usually lower than the cellular phone requirement, because of the large common mode IM2 ($\mathrm{IM2_{CM}}$) current generated in the pseudodifferential transconductor. As it is shown in the following equation, this CM current ($I_{\mathrm{IM2,CM}}$) is converted to differential products by the LO switching pairs asymmetry and load mismatch and is added to the other differential IM2 current [the first term of (1)] and appeared in the output IM2 current of the mixer ($I_{\mathrm{IM2,out}}$)

$$I_{\mathrm{IM2,out}}^2 = L^2 I_{\mathrm{IM2,diff}}^2 + \left(L^2 + \left(\frac{\sigma_R}{R_L}\right)^2\right) I_{\mathrm{IM2,CM}}^2 \quad (1)$$

in which $I_{\mathrm{IM2,diff}}$, R_L, σ_R, and L are the differential IM2 current generated in the transconductor, the mixer output resistance, standard deviation of output load, and low-frequency leakage of the switching transistors, respectively.

B. Proposed Calibration Technique

The $\mathrm{IM2_{CM}}$ current, generated in the pseudodifferential input stage, is proportional to the $\mathrm{g_2}$ i.e., the second-order coefficient of the MOS *I–V* characteristic [8]

$$I_{\mathrm{IM2,CM}} \propto \frac{g_2}{2}. \quad (2)$$

The $\mathrm{IM2_{diff}}$ current of pseudodifferential transconductor is mainly due to the variation in the threshold voltage as below [8]

$$I_{\mathrm{IM2,diff}} \propto \frac{3g_2}{4(V_{\mathrm{gs}} - V_{\mathrm{TH}})}\sigma_{V_{\mathrm{TH}}} \quad (3)$$

in which V_{gs}, V_{TH}, and $\sigma_{V_{\mathrm{TH}}}$ show the gate–source voltage, threshold voltage and the standard deviation of V_{TH}, respectively.

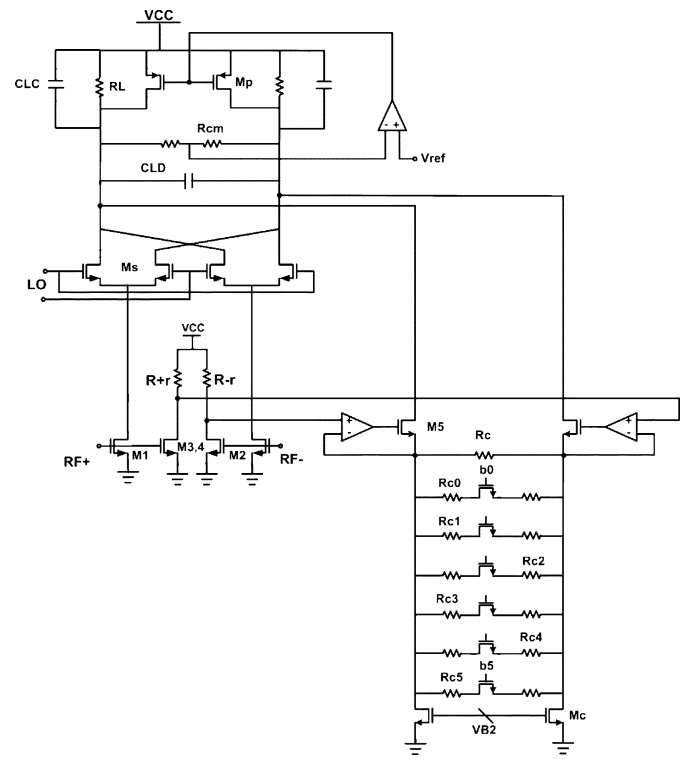

Fig. 3. Proposed calibrated mixer.

By using (2) and (3)

$$\frac{I_{\mathrm{IM2,diff}}}{I_{\mathrm{IM2,CM}}} = \frac{3\sigma_{V_{\mathrm{TH}}}}{2(V_{\mathrm{gs}} - V_{\mathrm{TH}})}. \quad (4)$$

By assuming $V_{\mathrm{gs}} - V_{\mathrm{TH}} = 100$ mV and $\sigma_{V_{\mathrm{TH}}} = 2$ mV, this ratio is 0.03.

The CM and differential IIP2 of a pseudodifferential transconductor versus biasing current is shown in Fig. 2. Since, IIP2 is reversely proportional with IM2 current, it can be concluded that in this transconductor, the $\mathrm{IM2_{CM}}$ current is more powerful than $\mathrm{IM2_{diff}}$ current by more than one order of magnitude. This can be written as below

$$\left(\frac{I_{\mathrm{IM2,diff}}}{I_{\mathrm{IM2,CM}}}\right)^2 = \alpha^2 \ll 1. \quad (5)$$

Moreover, considering a pessimistic value for L and σ_R such as -40 dB in (1), it can be found that $\mathrm{IM2_{diff}}$ current at mixer output is much lower than $\mathrm{IM2_{diff}}$ current at transconductor output. Therefore, a good idea for canceling differential IM2 current at the mixer output is converting the $\mathrm{IM2_{CM}}$ current of transconductor to the differential part and then injecting it to the mixer output after attenuation. As the proposed calibration system is shown in Fig. 1, an IM2 generator block senses the input RF blockers, generates the $\mathrm{IM2_{CM}}$ current and converts it to the required differential IM2 components which is controlled by a programmable operational transconductance amplifier (OTA) and is injected to the mixer output. Referring to Fig. 3, the IM2 generator is made by M3 and M4 transistors which are in parallel with mixer input transistors (M1, M2).

The analytical analysis of the proposed calibration technique is as below.

Referring to (1), the relationship between differential IM2 current at the uncalibrated mixer output ($I_{\mathrm{IM2,out}}$) with $\mathrm{IM2_{CM}}$ current generated in the mixer input stage can be simplified as below by considering (5)

$$I_{\mathrm{IM2,out}} = I_{\mathrm{IM2,CM}}\sqrt{L^2(1+\alpha^2)+\frac{\sigma_R^2}{R_L^2}}. \tag{6}$$

For the CMOS transistors in the strong inversion region the g_2 is

$$g_2 = \frac{2}{I}\left(\frac{gm}{1+\theta v_{\mathrm{od}}}\right)^2 \tag{7}$$

where V_{od} and θ are overdrive voltage and fitting parameter for mobility, respectively [9].

Since transistor M3 and M1 are in parallel in the input but with different biasing and sizing, by using (2) and (7) it can be found that the $\mathrm{IM2_{CM}}$ current generated in M3 transistor is proportional to that of M1 transistor. This is shown as below

$$I_{\mathrm{IM2,CM,M3}} = \beta I_{\mathrm{IM2,CM,M1}}. \tag{8}$$

Suppose that $\mathrm{IM2_{CM}}$ current of M3 and M4 transistors is converted to differential and is injected to the mixer output

$$I_{\mathrm{IM2,inj}} = -(gm_{\mathrm{Cal}}\cdot r)I_{\mathrm{IM2,CM,M3}} \tag{9}$$

in which $I_{\mathrm{IM2,inj}}$ is the injected current and other terms show the CM to differential conversion gain. The gm_{Cal} is the OTA transconductance and r shows the desired mismatch between load resistance of M3 and M4 transistors.

Considering (6) and (9), the $\mathrm{IM2_{diff}}$ current in the output of the calibrated mixer ($I_{\mathrm{IM2,out,Cal}}$) is

$$I_{\mathrm{IM2,out,Cal}} = I_{\mathrm{IM2,CM}} \times\left(\sqrt{L^2(1+\alpha^2)+\frac{\sigma_R^2}{R_L^2}}-\beta\cdot gm_{\mathrm{Cal}}\cdot r\right). \tag{10}$$

Therefore, it can be concluded that the IM2 cancellation in the output of the mixer can happen if the following condition is met:

$$gm_{\mathrm{Cal}} = \frac{\sqrt{L^2(1+\alpha^2)+\left(\frac{\sigma_R}{R_L}\right)^2}}{\beta\cdot r}. \tag{11}$$

C. Circuit Implementation

The proposed calibration technique is implemented as it is shown in Fig. 3. The required $\mathrm{IM2_{CM}}$ current, generated by an IM2 generator, is converted to differential by the desired mismatch between the load resistors of IM2 generator. The output of the IM2 generator is connected to a highly linear OTA stage.

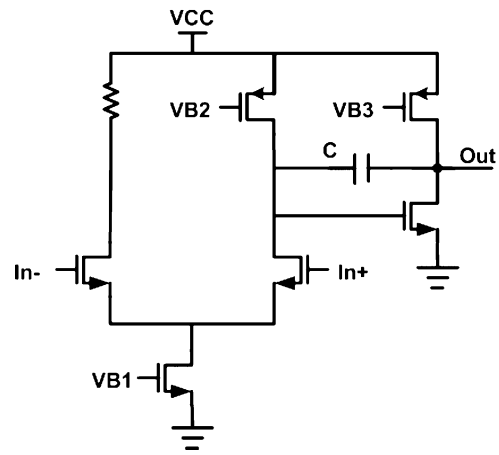

Fig. 4. Two-stage amplifier used in the input of OTA.

Since resistors are more linear than MOS transistors biased in the triode region, a resistor is chosen as the voltage to current converter in the OTA. This resistor determines the value of transconductance of the OTA as below

$$gm_c = \frac{1}{R_c}. \tag{12}$$

To achieve programmability in the OTA, this resistor is implemented by a fixed resistor (R_c) shunted with some switched resistors controlled by a six-bit control word ($\mathrm{b_0}-\mathrm{b_5}$). These control bits provide enough margins to fix PVT variations.

To avoid the nonlinearity of the OTA input transistors two opamps, which are two-stage Miller compensated amplifiers, are employed as it is shown in Figs. 3 and 4.

The bandwidth of the calibration circuit is dominated by the input stage of the OTA. The gain–bandwidth (GBW) of the OTA input stage is higher than 10 MHz because of using opamp with about 20-MHz GBW in a unity gain feedback. The second pole of the loop is in the source node of M5 transistor which is very far from the first pole.

To cancel the all IM2 components in the signal channel, the calibration circuit bandwidth should be higher than half of the signal bandwidth in a zero intermediate frequency (IF) receiver. Therefore; the proposed calibration circuit can works for high channel bandwidth applications like UMTS and IEEE802.11 with about 4- and 20-MHz channel bandwidth as well as Global System for Mobile Communications (GSM) with 200 kHz.

The minimum supply voltage of the proposed circuit is equal to $V_{\mathrm{TH}}+3V_{\mathrm{od}}$, in which V_{TH} is the threshold voltage of nMOS Transistors. This minimum voltage is less than 1 V when V_{TH} is less than 0.5 V and V_{od} is considered 150 mV.

The temperature variation is an issue for all calibration circuits. A general solution for this kind of variations is based on sensing the temperature effect in the calibration circuit and adjusting the proper calibration code by considering the temperature variation effect. This adjustment is done in [4] by varying the temperature coefficient of the resistors. Since a LMS feedback algorithm in which the calibration is updated periodically should be employed to adjust the calibration [3], therefore, the

temperature and other low speed variations can be compensated if the calibration code setting is updated every few seconds.

D. Noise in the Calibrated Mixer

The main problem of the differential calibration is the flicker and thermal noises of the calibration circuit which are injected directly to the mixer output. Moreover, in cellular phone applications and especially GSM there is tough requirement on the noise performance which is mainly degraded by flicker noise of the mixer. Therefore, the noise of the calibration circuit should be highly lower than mixer noise in order not to degrade the mixer noise figure (NF).

Considering the thermal noise, the noise of calibration circuit seen in the output of the mixer is

$$v_{n1,\mathrm{Cal}}^2 \approx 8KT\left(\gamma gm_3\frac{R^2}{R_C^2}+\frac{1}{R_C}+\gamma gm_5+\frac{v_{n,\mathrm{Op}}^2}{R_C^2}\right)R_L^2 \tag{13}$$

in which, the terms from the first to the last are the noise of M3 transistor, R_C resistor, M5 transistor and opamp, respectively. Moreover, γ is the channel noise factor which is 2/3 for long channel MOS transistors. The noise of resistor R (the load of M3 and M4 transistors) can be neglected because

$$R \ll R_C. \tag{14}$$

Moreover, the thermal noise of R_C is also reduced by choosing R_C highly larger than R_L

$$R_C^2 \gg R_L^2. \tag{15}$$

Increasing R_C leads to lower CM to differential conversion gain in IM2 generator and OTA which is equal to r/R_C. However this can be compensated by increasing r.

By using (13)–(15), it can be shown that the M5 transistor has the main contribution in the thermal noise of calibrating circuitry.

The thermal noise of the uncalibrated mixer which mainly is dominated by input transistors is [10]

$$v_{n,\mathrm{mix}}^2 \approx 8KT\left(\frac{1}{R_L}+\gamma gm_1+\gamma\frac{2}{\pi}\frac{I}{A}\right)R_L^2 \tag{16}$$

in which A is the LO amplitude and I is the bias current of input transistors.

Therefore, considering main noise sources in (13) and (16), the thermal noise in calibrating circuitry is negligible comparing to uncalibrated mixer, if the following equation is met:

$$gm_5 \ll gm_1 \tag{17}$$

which it can easily be satisfied because, firstly the bias current of M5 transistor is much lower than that of the input RF transistors and secondly the channel length of M5 transistor is highly larger than the channel length of M1 transistor which acts as a RF transistor and its size is limited due to low requirement in input capacitive load of the mixer.

Regarding the flicker noise, the noise of the calibration circuit seen at the mixer output is as below

$$v_{n2,\mathrm{Cal}}^2 \approx 2\left(v_{n,M3}^2 gm_3^2\frac{R^2}{R_C^2}+v_{n,M5}^2 gm_5^2+\frac{v_{n,\mathrm{Op}}^2}{2R_C^2}\right)R_L^2 \tag{18}$$

in which, the main flicker noise contributors including M3 transistor, M5 transistor and opamp $(v_{n,M3}^2, v_{n,M5}^2, v_{n,\mathrm{Op}}^2)$ are considered.

The flicker noise of M3 transistor is reduced by lowering the biasing current and using non minimum size channel length, while in M5 and opamp it is achieved by lowering bias currents and increasing the area of transistors. By this strategy, the low noise performance in opamp can be achieved without affecting the gain and bandwidth requirements.

III. Proposed Mixer

A mixer, enhanced by the proposed cancellation technique, for UMTS applications is designed as it is shown in Fig. 3. The M1 and M2 transistors, sized by 120μm/0.15μm, are biased by 2 mA. The size of M3 and M4 transistors (input stage of IM2 generator) is chosen 10μm/0.15μm which is lower than the size of M1 and M2 transistors in order to achieve less noise and capacitive load, as it was mentioned. M3 and M4 transistors are biased each by 0.15 mA and connected to 100- and 200-Ω resistors. The OTA resistor R_C is chosen 2 kΩ. The OTA input stage transistor is biased by 0.3 mA and is sized as 160 μm/1μm.

The switching transistors are derived by a local oscillator with 5-dBm power and are sized by 400μm/0.24μm in order to achieve the optimum flicker noise and IIP2 performance.

Two pMOS transistors (Mp) with long channels are responsible for providing biasing current in the mixer output. Two *RL* resistors are also shunted with Mp transistors for reduction of their bias current and achieving lower voltage headroom. The common-mode (CM) and differential filtering in IF is done by *CLC* and *CLD* capacitors. A CM feedback (FB) loop made by a single-stage amplifier is employed to set the dc output voltage of the mixer.

IV. Simulation Results

The design was done in a 65-nm CMOS technology with 1-V supply. The IIP2 simulation is done by applying the worst case mismatches, equal to 3 times of the standard deviation mismatch (σ), to all transistors [5], [8]. These mismatches are calculated based on the process information and are verified by Monte Carlo simulations.

The IIP2 simulation is done by two-tone test at 1.98 GHz with different spacing less than 10 MHz which emulates the TX leakage as the main blocker while the LO frequency is 2.11 GHz. The Monte Carlo simulation of the calibrated and uncalibrated mixer is depicted in Fig. 5. It shows that the IIP2 of the proposed mixer is higher than 80 dBm which is higher than the cellular phones requirement (75 dBm), while in the conventional mixer it is between 55 and 75 dBm. Moreover it shows that the mixer achieves more than 25 dB improvement in IIP2.

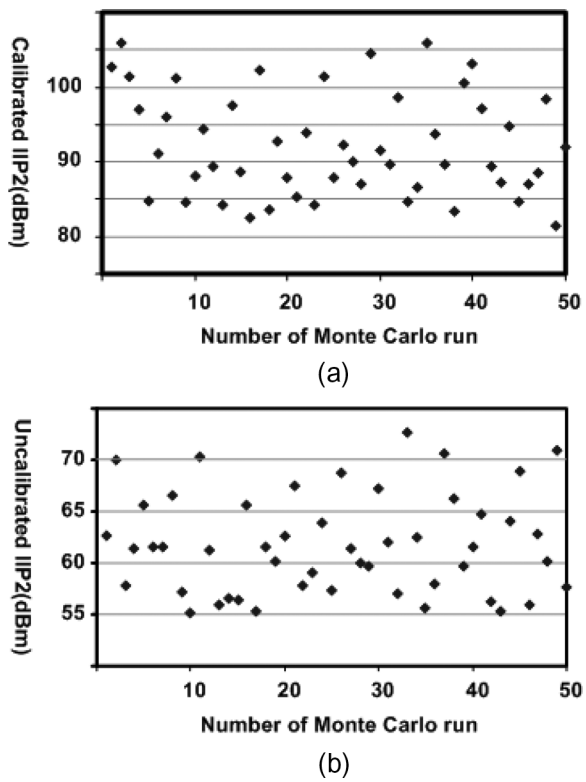

Fig. 5. (a) Result of Monte Carlo analysis of the enhanced mixer. (b) Rresult of Monte Carlo analysis of the conventional mixer.

The input-referred noise which is in band-averaged noise (10 kHz–1.92 MHz) is less than 3.8 nV/sqrt(Hz). The mixer NF performance in both calibrated and uncalibrated modes is shown in Fig. 6.

The third-order nonlinearity is simulated with the transmitter signal leakage inter-modulating with a blocker which is 67.5 MHz away from the receive band. The mixer IIP3, conversion gain and power consumption are 7 dBm, 12 dB, and 6 mW, respectively.

V. Conclusion

A new IIP2 calibration technique for zero-IF mixers is presented. The technique is based on injecting a nonlinear current to the mixer output. This current is made in an IM2 generator and is controlled by an OTA. Making use of this technique more than 25-dB improvement in the mixer IIP2 is achieved. The mixer meets the tough cellular phone IIP2 requirement. The calibration circuit is designed to be low noise in order not to degrade the mixer NF. The design works with supplies as low as 1 V and has enough bandwidth for high channel bandwidth applications like UMTS and IEEE802.11 as well as GSM; therefore it is a good candidate for high IIP2 multistandard mixers. The linearity performance of this mixer goes toward the demand of fully integrated, hardware shared universal mobile terminal.

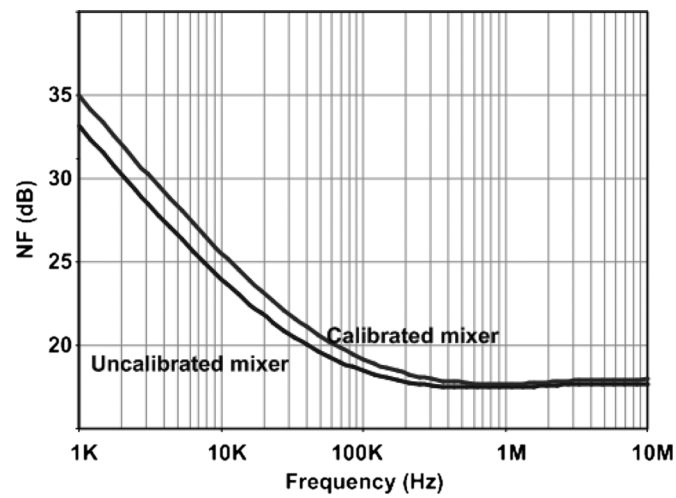

Fig. 6. NF in calibrated and uncalibrated mixers.

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