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A 2-15 GHz VCO With Harmonic Cancellation for Wide-Band Systems

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***Abstract*—A 2-15 GHz SiGe VCO (voltage controlled oscillator) has been developed with a very low harmonic content. The design is based on the harmonic cancellation concept and uses a multiple-phase ring oscillator together with a wide-band active-weighted summer. The VCO results in an output power of −8 to −6 dBm and < −50 dBc 3rd and 5th harmonic level at 2-15 GHz. The active area of the chip is very small (0.67 × 0.25 mm^2) due to the lack of inductors, and the power consumption is 88-120 mW from a 2.5 V supply. To our knowledge, this is the first demonstration of a wide-band VCO showing a near-perfect sinewave output over a wide frequency range. The application areas are in built-in-self-test sources for wide-band radios and phased arrays.**

***Index Terms*—BIST, harmonic cancellation, ring oscillator, SiGe, wide-band VCO.**

I. Introduction

THE generation of wide-band signals has been a challenge for several years, and is typically based on: a) a VCO or two VCOs covering an octave band followed by frequency multipliers such a doublers and triplers [1], b) a high frequency VCO followed by a set of dividers, and c) wide-band ring oscillators [2], [3]. The VCO+multiplier chain results in low phase noise, but requires a large number of passive filters to remove the multiplier harmonics. Alternatively, the VCO+divider chain also results in low phase noise, but suffers from high harmonic levels due to the divider square-wave output (−10 dBc for the 3rd harmonic). The wide-band ring oscillator also results in a high harmonic levels again due to the near square-wave output of these circuits. Therefore, there are no compact circuits which can generate a wide-band signal with low harmonics and without the use of on-chip or external low-pass or bandpass filters.

This letter presents a wide-band ring VCO with harmonic cancellation. The idea is based on a technique used in harmonic-rejection mixers, typically referred to as phase-weighted cancellation [4]. The VCO is built in a SiGe BiCMOS process, and achieves <−50 dBc 3rd and 5th harmonic levels at 2-15 GHz. The same design technique can also be used in a CMOS process, and in VCO+divider chains as well.

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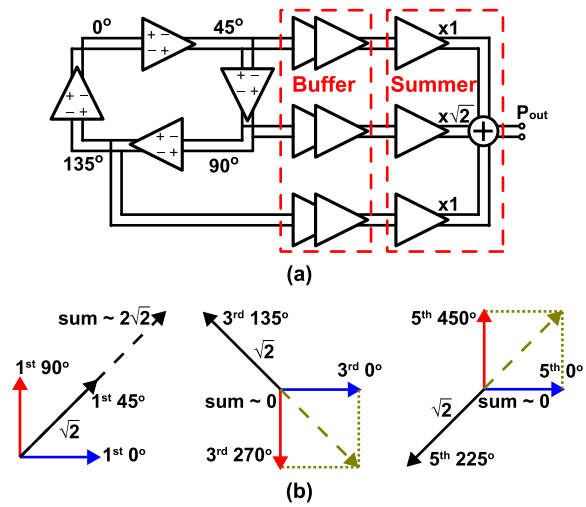

Fig. 1. Harmonic-cancellation architecture based on a multiple phase ring oscillator.

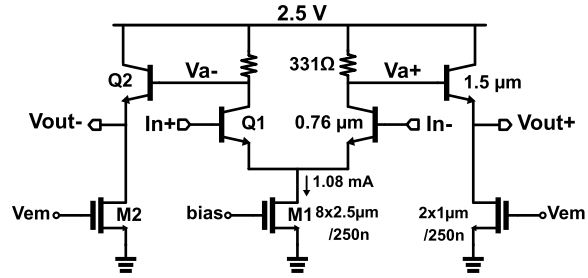

Fig. 2. Differential core delay-cell of the ring VCO.

II. Design

The harmonic cancellation VCO architecture is shown in Fig. 1(a). The circuit is designed in Jazz SiGe BiCMOS H3 process with an f_t of 220 GHz and six metal layers. No inductors are employed since the wide-band VCO is to be used in built-in-self-test systems and should occupy a very small chip area. A differential SiGe ring VCO with outputs at 45°, 90° and 135° is designed using core transistor pairs followed by emitter follower stages, and the three outputs are combined together in a wide-band active summer with a 1:$\sqrt{2}$:1 weighting factors, respectively. This weighting results in a 3rd and 5th harmonic cancellation and is the backbone of harmonic-cancellation mixers [4] (Fig. 1(b)).

Fig. 2 presents the ring oscillator delay-cell core with MOS transistors for the current control and BJT transistors for the g_m delay-cells and emitter followers [5]. For a ring oscillator

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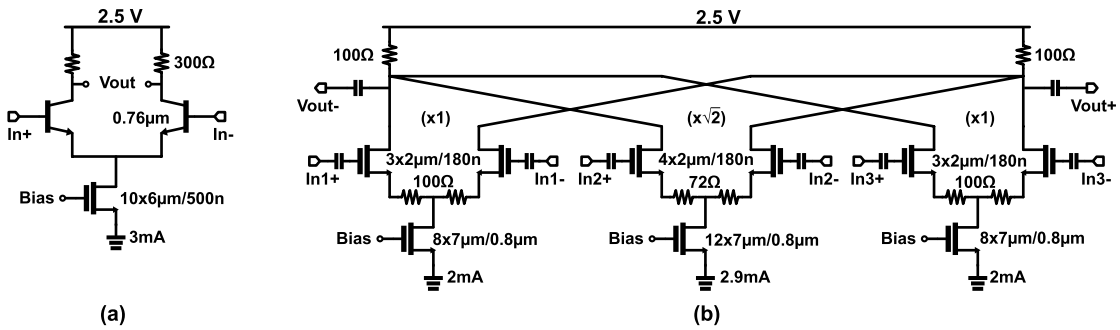

Fig. 3. (a) Buffer stage, and (b) weighted summer with resistive degeneration.

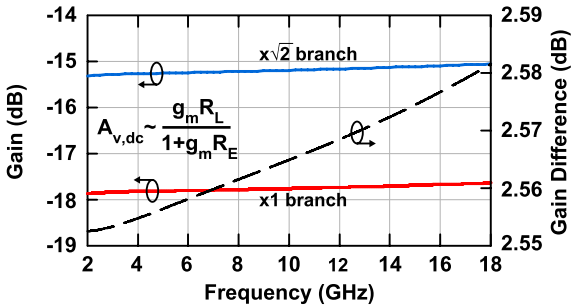

Fig. 4. Simulated gain and gain difference of current combiner's weighted branches.

with n stages, the oscillation frequency is determined by the two poles at the V_{out} and V_a nodes and is given by:

$$\omega_o = -\frac{\omega_{p1}+\omega_{p2}}{2k} + \frac{1}{2}\sqrt{\left(\frac{\omega_{p1}+\omega_{p2}}{k}\right)^2 + 4\omega_{p1}\omega_{p2}} \quad (1)$$

where $k = tan(\frac{\pi}{n})$. For a four-stage oscillator, the widest tuning range is achieved if the V_{out} pole is set to be dominant. Frequency tuning is realized by controlling the Q2 bias current, which shifts the V_{out} pole depending on the corresponding Q2 g_m value. For a tuning range of 2-15 GHz, the Q2 g_m is changed from $\sim$ 0.25 mS to $\sim$ 65 mS by controlling the current in M2 (7 μA-1.6 mA). The ring oscillator employs 4 delay cells and consumes 4.4-17 mA for 2-15 GHz operation. The 45°, 90° and 135° outputs are followed by two wide-band resistively-loaded buffer stages with a voltage gain of 12-2 dB versus frequency at 2-15 GHz (Fig. 3(a)), and then fed into a 0.18 μm CMOS active summer (Fig. 3(b)). In order to obtain a wide-band weighting of $\sqrt{2}$, different transistor sizes and bias currents are chosen for the x1 and x$\sqrt{2}$ paths, along with weighted emitter degeneration. Fig. 4 presents the simulated gain difference between the weighted branches. The voltage gain of the branches is kept constant over a wide frequency by the proper choice of DC blocking capacitors at the summer input and the output ports. The small-signal gain difference is optimized at 2.57 dB instead of 3.0 dB for the best harmonic cancellation by compensating for the non-linearity effects of the other active components. The differential summer output impedance is 200 Ω at 2 GHz and drops to 118 Ω at 15 GHz due to the transistor loading capacitance.

A microphotograph of the harmonically clean VCO is shown in Fig. 5. Note that the transmission-line connections between the three identical buffers and the summer are of equal

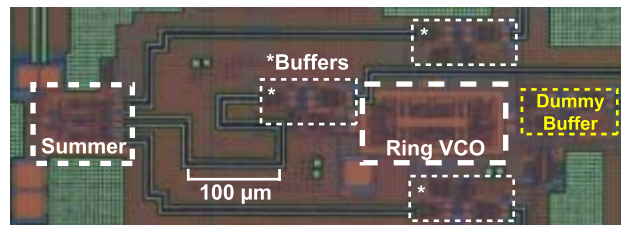

Fig. 5. Chip photo of the ring VCO with the weighted summer: 0.67 × 0.25 mm^2. (Dummy buffer is turned on for uniform loading.)

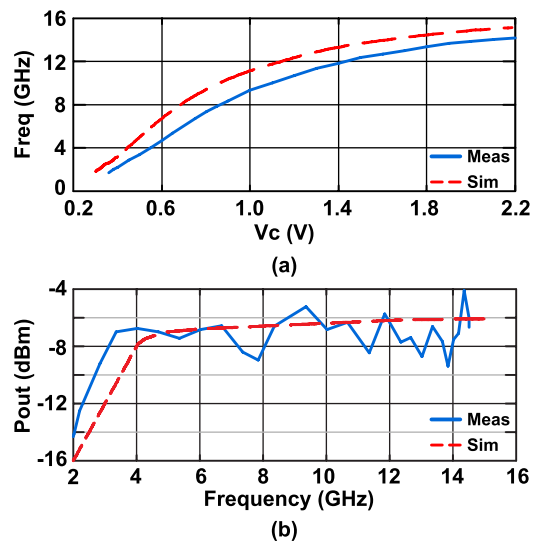

Fig. 6. (a) Measured and simulated output frequency, and (b) power level.

electrical lengths so as to maintain the same phase difference in all paths. The active circuit area is 0.67 × 0.25 mm^2, and the entire VCO consumes 88-120 mW from a 2.5 V supply. This power is relatively high due to the resistively loaded stages and the wide-band VCO operation. However, in most applications, the VCO will be turned on for a short time for built-in-self-test routines and therefore, the power consumption is not critical [6]. Calibre RC-extraction is used up to metal 4, and EM modeling by Sonnet EM-Suite is used at the upper metal levels.

III. Measurements

The harmonically-clean VCO is designed with a 200 Ω load so as to feed other circuitry in a wide-band chip. The same ring VCO is used in a break-out cell and connected to a 50 Ω GSSG probes for measurements. The measured VCO tuning range and output power are shown in Fig. 6 and

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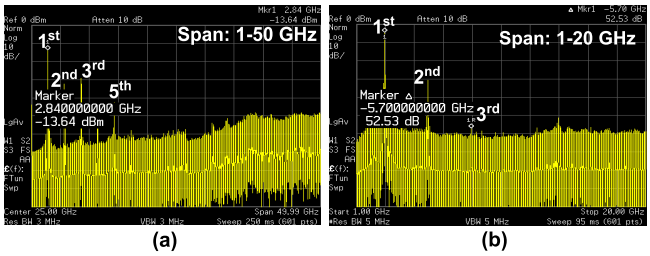

Fig. 7. Spectra for: (a) Single-phase output w/o harmonic cancellation at 2.84 GHz, and (b) 2.84 GHz signal showing 3rd harmonic suppression at 8.52 GHz.

TABLE I

VCO MEASURED OUTPUT HARMONIC CONTENT

	Harm. Cancelled		Single VCO Out	
Fund. Freq. (GHz)	3rd Harm. (dBc)	5th Harm. (dBc)	3rd Harm. (dBc)	5th Harm. (dBc)
2.84	-52.3	n.d.	-18.1	-30.3
3.42	-57.9	n.d.	-14.0	-30.2
4.11	-58.6	n.d.	-15.3	-32.7
4.83	-53.7	n.d.	-17.0	-33.9
6.68	<-60	n.d.	-21.9	-39.3
8.34	<-60	n.d.	-21.2	-38.4
10.67	<-60	n.d.	-23.0	o.r.
n.d.: not detectable, o.r.: out-of-range				

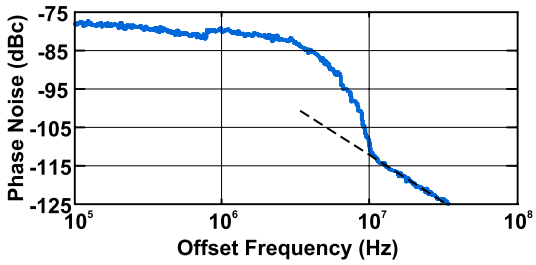

Fig. 8. Measured phase noise vs. offset frequency at 14.72 GHz.

agree well with simulations. A constant output power of -8 dBm is achieved from 3-15 GHz including the wide-band 100 Ω to 50 Ω impedance mismatch. Fig. 7(a) presents the spectrum of a single output for the ring-oscillator at 2.84 GHz, and the high harmonic levels are clearly seen. Note that due to the wide-band nature of the measurement system, single-ended measurements are done and therefore, the 2nd harmonic content is present, but this cancels out in a differential system. The output spectrum after the weighted summer is shown in Fig. 7(b) and (c), and the 3rd harmonic level is <-50 dBc (2nd harmonic is again due to the single-ended measurements).

Table I presents detailed measurements for the 3rd and 5th harmonic levels. The harmonic-cancellation technique lowers the 3rd and 5th harmonic levels by >30 dB as compared to a non-weighted output over a wide frequency range. The dynamic range of the harmonic level measurements is limited by the jitter characteristics of the free-running VCO. Frequency drift due to the jitter sets a relatively high minimum value for the resolution bandwidth, and it increases the noise floor of the spectrum analyzer.

TABLE II

PERFORMANCE SUMMARY & COMPARISON

	Freq. (GHz)	Out. Pow. (dBm)	Pow. Cons. (mW)	Phase Noise (dBc)
This work	**2-15**	**-6 to -8**	**88-120**	**-112 (10 MHz)**
[3] (SiGe)	8-17	-15	115	-
[7] (InP)	14-22	-4	130	-90 (1 MHz)
[2] (CMOS)	3-11	-1	-	-110 (10 MHz)
[8] (SiGe)	5-9	-9 to -14	40-94	-70 (1 MHz)

The measured phase noise around 14.72 GHz is shown in Fig. 8. The usual phase noise behavior is not observed until 10 MHz offset due to frequency drift of the free-running oscillator. The ring-based VCO results in a relatively high phase noise, but is adequate for built-in-self-test systems. The phase noise is comparable to, if not better than, published work (Table II).

IV. CONCLUSION

A wide-band SiGe ring VCO showing a near-perfect sine-wave over a wide frequency range is demonstrated using weighted summing. The harmonically-clean spectrum makes it suitable for wide-band testing systems, such as built-in-self-test for wide-band transceivers and phased arrays. To the best of our knowledge, this is the first demonstration of harmonic cancellation technique in wide-band integrated oscillators at microwave frequencies.

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