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SHORT PAPER

Pass Transistor-Based Pull-Up/Pull-Down Insertion Technique for Leakage Power Optimization in CMOS VLSI Circuits

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Abstract Reduction in leakage power consumption is one of the important issues in the field of VLSI. Numerous techniques have been proposed by several researchers, based on threshold voltage variations and gate modifications. In this paper, a novel pass transistor-based pull-up/pull-down insertion technique is proposed to minimize standby leakage. Experimental results on various ISCAS'89 benchmark circuits show that proposed technique has an improvement up to 20, 36 and 33 % on average in leakage reduction, delay improvement and area savings respectively, compared to the transmission gate-based technique. All benchmark circuits are simulated using H-spice Tool with an 180-nm standard cell library based on BSIM3 transistor model. Finally, the efficacy of the proposed approach in improving various metrics has been compared with present state-of-art methods.

Keywords Leakage power · Pass transistor · Transmission gate · Low power

1 Introduction

Dynamic power has dominated the total power consumption in the past. However, with the upgrading trend in technology, static power reins the total power consumption in VLSI circuits. Power dissipation in CMOS circuits is mainly categorized into dynamic power and static power. Dynamic power is the power consumption due to switching of

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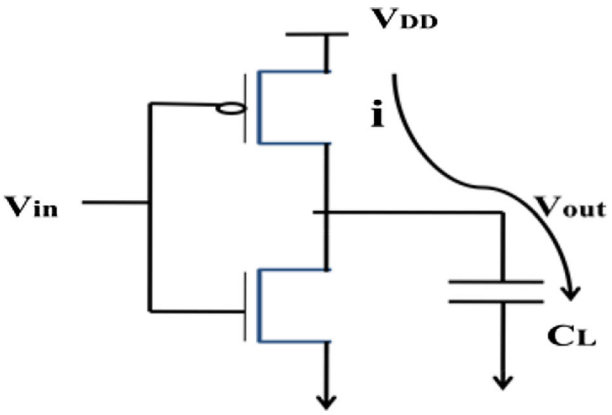

Fig. 1 Dynamic power dissipation in CMOS inverter

MOS transistors. Dynamic power dissipation in a CMOS inverter circuit is depicted in Fig. 1. This illustrates charging and discharging paths of load capacitor C_L through internal ON resistances of PMOS and NMOS transistors.

Dynamic power can be expressed as

$$P_{\text{dynamic}} = \alpha . C_L . V_{DD}^2 . f_{\text{clk}} \tag{1}$$

where α is the switching activity, C_L is the Load capacitance, V_{DD} represents Supply voltage and f_{clk} is the Clock frequency. Reducing the supply voltage is a successful method to reduce dynamic power. Static power is the power consumption when transistors are in the idle state. Ideally, there should be no power consumption in the idle state. However, internal leakage currents in MOS transistors result in static power. Static Power can be expressed as given by Eq. (2)

$$P_{\text{static}} = V_{DD} . I_{\text{leakage}} \tag{2}$$

where P_{static} is the static power consumed, V_{DD} is the supply voltage and I_{leakage} represents an internal leakage current. Equation (2) illustrates that reducing the supply voltage is one of the techniques to reduce static power. Decreasing the leakage current is also an effective way of minimizing the static power in standby mode. Out of various leakage sources, subthreshold leakage is a dominant source which leads to rise in static power. This can be expressed as given by Eq. (3)

$$I_{\text{subthreshold}} = I_0 \, e^{\frac{(V_{gs} - V_{th})}{\eta V_T}} \left(1 - e^{\frac{-V_{ds}}{V_T}} \right) \tag{3}$$

where $I_0 = \frac{W \mu_0 C_{0x} V_T^2 e^{1.8}}{L}$, V_{gs} and V_{th} represents a gate to source and threshold voltages respectively. V_{ds} is a drain-to-source voltage and V_T represents a thermal voltage constant. η is subthreshold swing coefficient and W, L are the width and lengths of a

transistor respectively. Cox is the gate oxide capacitance and μ_0 is the carrier mobility. Increasing the threshold voltage is one of the methods to reduce subthreshold leakage. Multiple techniques have been proposed in terms of threshold voltage variations and sleep transistor insertions [5,9,13,15]. The input vector control (IVC) technique is the one, which does not require any process modifications [1] unlike the previous mentioned techniques. The drawback of IVC technique is that it cannot be used for circuits with larger depth. The gate replacement technique is one of the best techniques used for leakage power reduction. Yaun et al. [19] in 2005 proffered an enhanced leakage reduction using gate replacement. They proved that the gate replacement technique can reduce additional 10–24 % leakage over traditional IVC method. Cheng et al. [3] in 2008 projected a simultaneous input vector generation and gate replacement algorithm for leakage power reduction, with better results than other traditional techniques. Gate modification is the disadvantage in the gate replacement technique. In [11] transmission gate-based approach is presented to minimize leakage power with an area and delay penalty. In this paper, a novel pass transistor-based pull-up/pull-down insertion technique is proposed. The proposed technique efficiently minimizes leakage power while reducing area and delay penalty. The rest of the paper is organized as follows: Preliminaries and motivation are presented in the Sect. 2 and proposed work is introduced in Sect. 3. The effectiveness of the proposed technique is evaluated in Sect. 4 and finally Sect. 5 concludes the paper.

2 Preliminaries and Motivation

In this section classical methods to minimize leakage power are reported briefly.

2.1 Leakage Reduction by Gating the Supply Voltage

Gating the power supply rails using sleep transistors is a well-known method formerly. Many researchers have introduced techniques [9,13,15] like sleep method, forced stack, sleepy keeper, etc. Park et al. [13] proposed sleepy stack method of combining sleep technique along with a stack method. Sleep transistors cut off the circuit from power supply rails, thereby reducing power consumption. Kaushik Roy et al. [15] propounded leakage reduction techniques in deep submicrometer CMOS circuits. The disadvantage with these techniques is the necessity of high-threshold sleep transistors. This requires extra process steps in the fabrication and adding sleep transistors leads to an area penalty.

2.2 Input Vector Control (IVC)

IVC methods were introduced by Halter and Najm [6] and Ye et al. [18]. The effect of input patterns on a leakage current was observed and analyzed in [6,18]. Stack of more "OFF" transistors in the circuit results in more effective resistance, and less leakage [19]. Finding out an input pattern which can consume minimum leakage is the foremost task in IVC approach [4]. Imposing the circuit to this minimum leakage state

Table 1 Leakage power values of three-input NAND gate

S. no	State	Leakage power (W)
1	000	36.85 f
2	001	154.77 f
3	010	92.79 f
4	011	5.73 p
5	100	955.96 f
6	101	5.44 p
7	110	6.08 p
8	111	15.72 p

Table 2 Leakage power values of two-input NAND gate

S. no	State	Leakage power (W)
1	00	154.77 f
2	01	5.73 p
3	10	5.44 p
4	11	10.48 p

during standby mode is the fundamental concept in IVC. Abdollahi et al. [2] presented IVC technique to reduce leakage current by finding Minimum Leakage Vector (MLV). The circuit is imposed by MLV to reduce power consumption during standby mode. Tables 1 and 2 shows leakage power values of three-input and two-input NAND gates measured using H-SPICE tool.

Table 1 shows "000" is MLV. Exhaustive circuit simulation is used to find this state. But this is not possible for larger circuits. Many researchers have used heuristic algorithms to determine this minimum leakage state. In [1] linear search method is used to obtain minimum leakage state. Further, they have introduced control point insertions to reduce leakage power. Chen et al. [4] proposed genetic algorithm to search for MLV. Authors in [10] used genetic algorithm to find minimum leakage state. Rjoub et al. [14] presented fast input vector control algorithm to find MLV.

2.3 Gate Replacement Algorithm

The main drawback of IVC is that it is not suitable for circuits with more number of cascading stages. In gate replacement, gates which are at Worst Leakage State (WLS) consuming more leakage current are identified and replaced by standard cell library gates as shown in Fig. 2.

Gate replacement technique replaces a logic gate named "Gate" with a "Gate_{new}" from the standard cell library. The concept of gate replacement is presented in the following steps.

1. Gate_{new} (I,0) = Gate(I) for sleep = 0 in active mode
2. Gate_{new} (I,1) $\neq$ Gate(I) for sleep = 1 in standby mode
3. Leakage { Gate_{new} (I,1)} $<$ leakage {Gate(I) } in standby mode

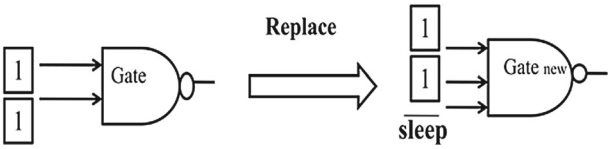

Fig. 2 Gate replacement of a NAND gate

where 'I' represents a gate input and $\overline{\text{sleep}}$ is an additional input connected during gate replacement. This additional input will not change the gate functionality during active mode, whereas in standby mode this input leads to leakage current reduction. As depicted in Fig. 2 gate input "11" changes to "110" with sleep = 1 during standby mode. This leads to a leakage reduction from 10.48 to 6.08 pW as presented in Tables 1 and 2. Many authors have proposed a combined effect of IVC and gate replacement to have better leakage reduction. A combined method of divide-and-conquer approach presented in [20] outperforms pure IVC in leakage savings by 24 %. A simultaneous input vector control and circuit modification is proposed by Jayakumar et al. [7].

Authors in [8] presented gate replacement in a slack-aware manner to minimize leakage along with zero delay penalties. Fast heuristic algorithm has been introduced in [3] to find low leakage vector and combined with gate replacement. Wang et al. [17] introduced direct gate replacement algorithm and divide-and-conquer-based gate replacement algorithm. Results show that algorithms outperform pure IVC by 15–30 % with 5 % delay relaxation. Modified gate replacement algorithm proposed by Singh et al. [16] in 2013 projects a method of moving away from those gates which increases other consequent "gates" leakages, contributing to overall leakage. The main drawback of the gate replacement technique is the gate modification needed for leakage reduction.

2.4 Transmission Gate (TG)-Based Technique

Instead of modifying the gate as in gate replacement algorithm, transmission gates along with the pull-down transistor are added in front of protected gates [11] to reduce leakage. Chao et al. [12] proposed TG-based technique in 2013 for leakage and negative bias temperature instability (NBTI) mitigation.

In Fig. 3 for active mode, sleep = 0 makes the transmission gate ON and drives pull-down NMOS transistor in to OFF state. This passes the output of gate 1 to the gate 2, whereas in standby mode, sleep = 1 sets the transmission gate to OFF state and input of gate 2 is pulled down to logic 0 for leakage reduction. In this technique, delay caused is independent of the gate type unlike gate replacement technique.

After identifying critical gates authors of [12] have inserted transmission gates in front of critical gates which require protection. Then, transmission gate insertion is carried out in non-critical gates. Though leakage reduction is achieved, inserting transmission gates in front of critical gates as well as non-critical gatesneeds more

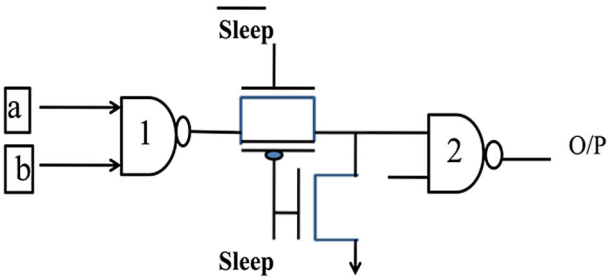

Fig. 3 TG-based technique for leakage reduction

area consumption and performance degradation. Hence, this led toward the proposed approach.

3 Proposed Pass Transistor-Based Pull-Up/Pull-Down Insertion Technique

This section introduces the proposed work. Unlike the techniques stated in the previous section, the proposed work protects every gate in the circuit without finding the critical gates. Later, the pass transistor-based pull-up/pull-down insertions is carried out in the proposed method. Some noteworthy points experimented in the proposed work on standard ISCAS'89 benchmark circuits which resulted in improved leakage reduction are given below:

1. Making every gate in the circuit at its best leakage state by inserting a transmission gate without finding critical gates ultimately reduces the overall leakage power of the circuit. However, this will increase area and delay penalty by considerably reducing standby power compared to the original circuit.
2. After taking into account the above point of area and delay penalty, authors have proposed a novel pass transistor-based pull-up/pull-down insertion technique. Absolutely, the proposed method is successful in minimizing area and delay penalty along with leakage reduction.

The implementation flow of the proposed technique in sleep mode is illustrated in Fig. 4. Initially node values of all gates are to be determined to identify gates with best leakage inputs. After identifying gates with the best inputs, they are left status quo and the worst and second-worst leakage state gates are checked. Pass transistor-based pull-up/pull-down insertion is applied to all these gates to make sure that the circuit consists of only best leakage inputs to all the gates. The logic structure of the proposed technique is depicted in Fig. 5.

From Fig. 5a it is observed that a PMOS pass transistor with the pull down has been added in front of gate 2, to make it as a best leakage state gate. Tables 3 and 4 present various modes that a circuit can operate with pull-up/pull-down insertions. When $X = 0$ and sleep = 0, pass transistor is in ON state and the pull down transistor is in OFF state. Hence, the circuit operates in active mode. During the standby mode, $X = 1$ cuts

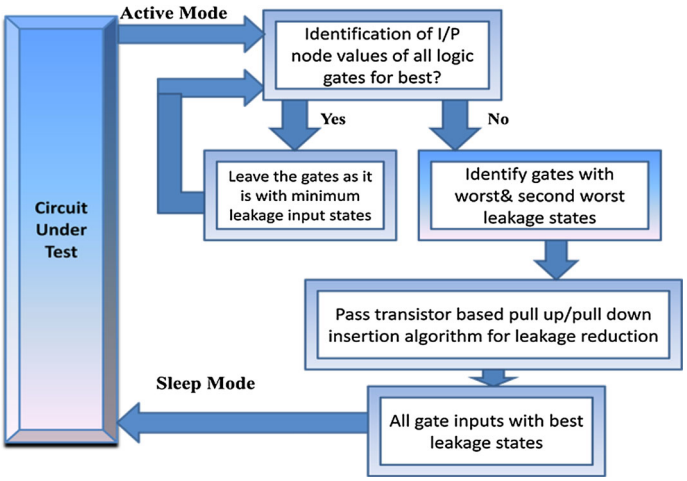

Fig. 4 Implementation flow of proposed technique in sleep mode

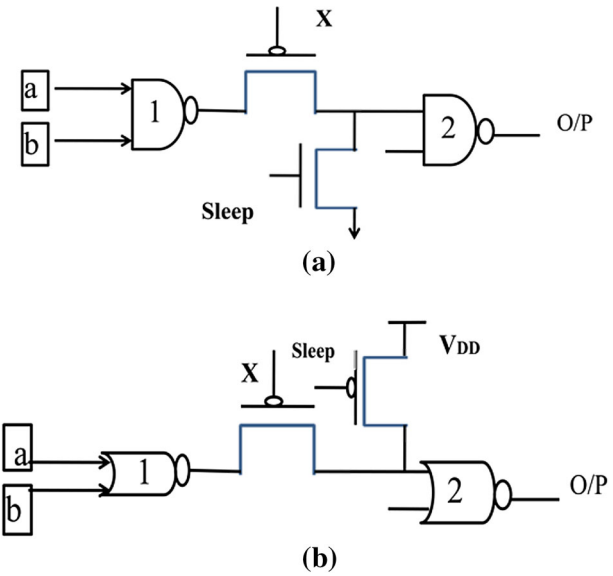

Fig. 5 **a** Proposed technique for leakage reduction in NAND Based Circuit. **b** Proposed technique for leakage reduction in NOR Based Circuit

Table 3 Modes of operation when pull down is inserted along with pass transistor

X	Sleep	Mode
0	0	Active
1	1	Standby

off the pass transistor and sleep = 1 turns on the pull down transistor. This makes the gate 2 input pull down to logic zero state.

Table 4 Modes of operation when pull up is inserted along with pass transistor

X	Sleep	Mode
0	1	Active
1	0	Standby

Algorithm: Pass transistor based pull up/pull down insertion algorithm

Input : { $gate_1$, $gate_2$ …. $gate_m$ }, m is the number of gates in a circuit

Calculate the internal node values of all gate inputs.
For i = 1 to m **do**
If $gate_i$ is already at best leakage state
then
No insertion for $gate_i$
else
Insert a pass transistor with pull down if $gate_i$ is of NAND type (or)
Insert a pass transistor with pull up if $gate_i$ is of NOR type.
Update new values of leakage and Delay after insertion
end
end

Fig. 6 Algorithm of proposed technique

As gate 2 is of NAND type, "00" is the best leakage state observed in Table 2 and is obtained using pass transistor with the pull down insertion. Similarly, for NOR gate structures, the best leakage state is "11" and is obtained using pass transistor with the pull up transistor as depicted in Fig. 5b. The circuits in Fig. 5 are made to operate in two conditions called active and standby mode. A simple PMOS pass transistor is used to interconnect gates during active mode. A PMOS transistor can pass a strong '1', so there are no issues in passing '1'. While passing logic '0', as PMOS transistor cannot pass strong '0', there is variation by V_{th} at the drain side of the PMOS pass transistor. Thus, the output at the PMOS pass transistor for logic '0' case is varied by V_{th} instead of having zero volts. As a single pass transistor is used, degradable logic values will not affect much in the cascading gates unlike the chain of pass transistors. The voltage at the output of PMOS pass transistor is within the acceptable limit of input voltage V_{IL} for gate 2.

Algorithm of the contributed work is described in Fig. 6. Input to the algorithm is 'm', representing the number of gates in the circuit. All nodes of the gates are checked for any requirement of pull up/pull down insertions. If the gate is already at minimum leakage state, then algorithm will continue with consecutive gates to search for the worst and second-worst leakage gates. Such gates are identified and are inserted with a set of pass transistor and pull up/pull down depending on the type of the gate. After the insertion, new values of leakage and delay are calculated. Now the test circuit is said to be in sleep mode with all gate inputs at the best leakage states, which can tremendously reduce leakage power compared to the original circuit and other existing methods.

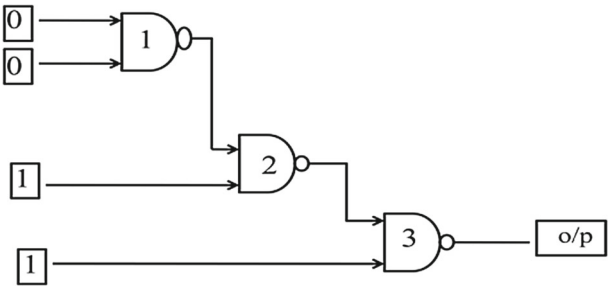

Fig. 7 Test circuit considered as an example

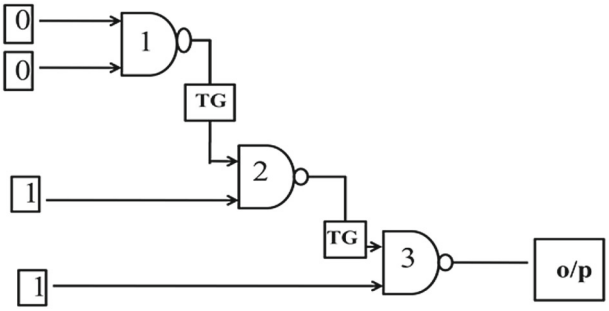

Fig. 8 TG-based technique applied to test circuit in Fig. 7

4 Implementation and Result Analysis

The algorithm of the proposed method is examined on all benchmarks and simulation results are presented. The concepts are analyzed using examples of Figs. 7 and 8. Table 2 shows leakage values of two-input NAND gate. Out of all input combinations "00" offers minimum leakage. Hence, if inputs of all NAND gates in the test circuit of Fig. 7 are imposed to this minimum leakage state in standby mode, total leakage power will be minimum.

From Fig. 7 it can be observed that gate 1 is at the best leakage state, gate 2 is at worst leakage state and gate 3 is at a second-worst leakage state. The total leakage power of the circuit is 16.364 pW. Fig. 8 illustrates that a transmission gate is inserted at the input of gate 2 which is identified as the Worst Leakage State gate. Hence, input of gate 2 has changed from "11" to "01," giving output as '1.' This gate 2 output is making gate 3 to be at Worst Leakage State. Hence, it is recommended to insert a Transmission gate at gate 3 input also. Apparently, gate 3 input changes from "11" to "01."

As gate1 is already at its best leakage state with "00," the total leakage power is now calculated to be 11.614 pW. Hence, except the gate 1, rest of the gate inputs are inserted with transmission gates. This has improved the leakage reduction to around 29 % compared to the original circuit. Hence, this method of inserting a transmission gate logic at every gate input in the circuit except gates with the best leakage states, has given satisfactory results. ISCAS'89 Benchmark circuits are used to test the technique. Later,

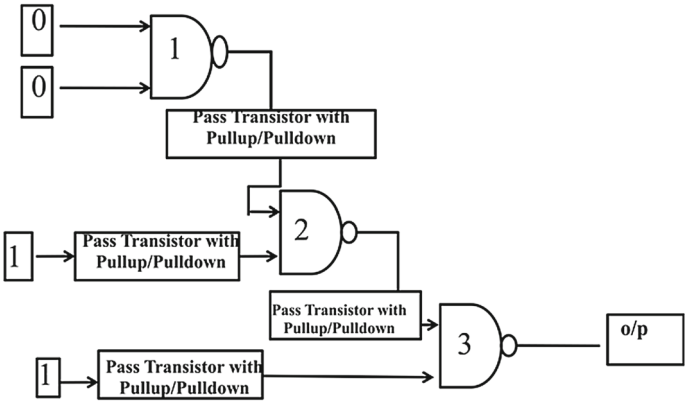

Fig. 9 Proposed technique applied to test circuit in Fig. 7

our experimentation has moved toward minimizing an area and delay penalty. Keeping this in view, a PMOS pass transistor-based pull-up/pull-down insertion technique has been proposed.

Figure 9 illustrates that the gate 1 is at its best leakage state. Hence, gate 2 and gate 3 inputs are inserted with pass transistor-based pull-down network. This makes all gate inputs in the circuit to be at the best leakage states. Thus, decreasing leakage power of the circuit from 16 pW to 462 fW reduces the leakage power by approximately 97 %. Circuit in Fig. 9 needs eight transistors, whereas the same circuit with the transmission gate insertions needs 12 transistors in addition to transistors used in gate 1, 2 and 3. Hence, our proposed technique has 33 % less area consumption. As less number of transistors is required with the proposed technique, leakage power and total path delay are ultimately reduced. Additional transistors used in the proposed method do not cause any thermal effects, because reducing the power dissipation with the proposed method in turn reduces heat dissipated by the chip. This may minimize usage of cooling techniques needed to reduce thermal effects. Hence, using low-power designs such as the proposed method reduces packaging and cooling cost required and increases chip reliability by minimizing thermal effects.

Different benchmarks of ISCAS'89 are used to validate the effectiveness of the proposed technique. Both combinational and sequential circuits are covered in test cases. Benchmarks contain all different kinds of gates. Benchmarks are simulated using HSPICE tool with an 180-nm standard cell library based on BSIM3 transistor model. Some key technology parameters are: $V_{dd} = 1.8$ V and $T_{ox} = 4.1$ nm. Table 5 shows leakage optimization of the proposed technique. Column 2 presents leakage values without any circuit modifications. Column 3 gives leakage values when proposed technique is applied for all test cases. Column4 presents 43.43 % improvement in leakage savings with respect to the original circuit. Though area and delay penalty exists compared to the base circuit, significant leakage savings up to 43.43 % is achieved on an average. Table 6 illustrates the experimental results of TG-based technique and the proposed technique. Column 2 and column 3 are the leakage power values when all gate inputs are imposed to the best inputs. Proposed pass transistor-based

Table 5 Leakage power comparison of proposed technique with original circuit

Benchmark circuit	Original leakage (W)	Proposed technique leakage (W)	% Improvement in leakage reduction
C17	3.183 p	2.01 p	36.79
S27	9.76 p	5.35 p	45.18
B02	13.56 p	13.08 p	3.53
S420	56.45 u	68.78 p	99
S641	150.08 p	101.02 p	32.68
Average improvement in leakage reduction			43.43

Table 6 Comparison between TG-based technique and proposed technique

Benchmark circuit	TG-based technique leakage (W)	Proposed technique leakage (W)	% Improvement in leakage reduction
C17	2.68 p	2.01 p	25
S27	7.03 p	5.35 p	23.89
B02	17.15 p	13.08 p	23.73
S420	87.22 p	68.78 p	21.14
S641	112.7 p	101.02 p	10.36
Average improvement in leakage reduction			20.82

pull-up/pull-down insertion technique outperforms TG-based technique in improving leakage reduction by 20.82 % on average.

Leakage savings are more in the proposed technique compared to TG based technique. There is a significant improvement in leakage savings beyond 20 % in test circuits C17, S27, B02, and S420 except S641. The reason for this is in S641 benchmark maximum gate inputs are already at the best leakage state resulting in less number of insertions and leakage savings up to 10 % only. The area estimation is made on the basis of number of insertions in both techniques. As the proposed technique requires only two transistors instead of three transistors in TG-based technique for every insertion, there is 33 % less usage of an area in the proposed technique. This ultimately reduces total delay in the circuit. Simulation results prove that the proposed technique outperforms other methods like TG-based techniques. Analysis has been performed based on device sizing also. In practice, leakage power can be reduced to a great extent based on device sizing because subthreshold leakage current I_{sub} is a function of device size. Subthreshold leakage decreases with the decrease in width (W) of the transistor. So, leakage power has been analyzed for different values of 'W' in the proposed method for all benchmarks. Leakage power estimation for a specific value of 'W' giving the least values of leakage power is taken as a case study and presented as results.

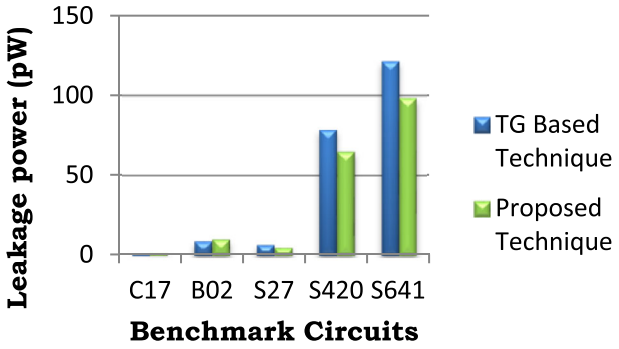

Fig. 10 Comparison between TG-based and proposed techniques

Table 7 Delay comparison of proposed technique with original circuit

Benchmark circuit	Original delay (s)	Proposed technique delay (s)	Delay overhead (%)
C17	1.881 n	3.499 n	46.24
S27	2.021 n	2.431 n	16.86
B02	3.068 n	5.0037 n	38.68
S420	3.861 n	4.955 n	22.07
S641	8.008 n	10.263 n	21.97
Average overhead in delay			29.16

Comparison of both techniques in terms of leakage power is explored in Fig. 10. Every gate is applied with its best leakage state in both the techniques. Results in Table 6 justifies that leakage power of the proposed technique has improvement in a leakage reduction up to 20 %. Delay in the circuit depends on the number of transistors including additional insertions caused by the proposed method. This may vary from one benchmark to others. More number of gates in critical paths leads to drastic delays. Table 7 projects delay overhead caused by the insertion of pass transistors in critical paths in the proposed technique compared to the original circuit. On an average there is a delay overhead of 29.16 % in the proposed technique with respect to the original circuit.

Table 8 illustrates delay comparison between TG-based technique and proposed technique. As the proposed technique requires less number of transistors compared to TG-based technique, there is a delay improvement of 36.869 % on average in the proposed technique. This in turn improves the performance of the circuit. Even in an S641 benchmark having 379 gates and 19 D-flip-flops (which is a large benchmark among the set of benchmarks validated) there is a delay improvement of 34.862 % compared to TG-based technique. Hence, outstanding experimental outcomes are recognized in the proposed method over counterparts in terms of leakage savings and delay improvements as illustrated in Tables 5, 6, 7 and 8 respectively.

As mentioned earlier, the number of transistors inserted in the total circuit is less in proposed technique and thus need approximately 33 % less area. Hence, the proposed

Table 8 Delay comparison between TG-based technique and proposed technique

Benchmark circuit	TG-based technique delay (s)	Proposed technique delay (s)	Delay improvement (%)
C17	2.578 n	3.499 n	26.321
S27	10.321 n	2.431 n	76.446
B02	7.498 n	5.0037 n	33.266
S420	10.132 n	4.955 n	51.095
S641	15.756 n	10.263 n	34.862
Average improvement in delay			36.869

technique has proved its effectiveness and outperforms other counter parts like TG-based technique in terms of leakage power, area, and delay.

5 Conclusions

Power, area, and delay are the major aspects of VLSI industry in the nanometer regime. In this paper, a novel pass transistor-based pull-up/ pull-down insertion technique is proposed which can reduce leakage power, area consumption and delay. Pass transistor-based pull-up/pull-down is inserted in front of every gate except the gates with the best leakage states.TG-based technique is also examined with all gate inputs at the best leakage states. Simulation results explores that proposed technique has achieved leakage reduction up to 20 % on average, delay improvement of 36.86 % and area minimization of 33 % compared to other state-of-art methods like TG-based techniques. Thorough investigation of the proposed method on various benchmarks proves that, insertion of a lesser number of transistors have achieved outstanding improvement in performance metrics. In future, the proposed method can be experimented with the latest technologies like below 90 nm and it can also be considered to mitigate the NBTI effect.

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