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On Designing All-Optical Multipliers using Mach-Zender Interferometers

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***Abstract*—In recent years, the design of all-optical circuits has received a great attention among the researchers due to high-speed and low-power characteristics and compatibility with CMOS technology. Some combinational logic circuits like adders, subtractors, multipliers, multiplexers, which are useful in optical communication network in data centers and high-perform computers, have been designed using optical components. There are two different design styles, called as *Design1* (based on conventional truth-table based approach) and *Design2* (based on binary decision diagram). In this paper, four different all-optical multipliers have been explored for array multiplier and carry save adder (CSA)-based multiplier based on these two design styles, using semiconductor optical amplifier (SOA) based Mach-Zender interferometers (MZIs). Simulation results confirm that MZI-based CSA multiplier (*Design1*) has the lowest optical cost and delay compared to those of other three multiplier designs (CSA multiplier - *Design2*, array multiplier - *Design1*, array multiplier - *Design2*) with a precision of 2 or more bits. Further, the proposed all-optical CSA multiplier designs outperform in terms of both optical cost and delay compared to the state-of-the-art designs of all-optical multipliers.**

I. Introduction

Although Moore's law has continuously dominated the VLSI industry during last five decades, this law is reaching to its limit as the increasing number of transistors cause more power consumption, which in turn dissipates more heat and loss of information in non-reversible circuits [1]. As a result, the current VLSI technology cannot be used to further reduce the size of the chip while controlling the heat dissipation. Several emerging technologies such as reversible computing, quantum computing and quantum photonics, etc. have been tried for circuit design to tackle this heat dissipation problem [2]. Among all these technologies, silicon-based optical computing (a.k.a., Si-photonics) has been experimentally demonstrated as one of the potential technologies for next generation computing [3]. Si-photonics is the combination of electronics and photonic circuits on a single chip that takes the advantages of both the technologies, viz., electronics and photonics. This is also most compatible with CMOS technology and has low fabrication cost with better performance compared to other technologies based on InP and TriPleX [3]. Among all reported researches, WIPE [4] is a project that aims to have both photonic integrated circuit (PIC chips) and electronic integrated circuit (EIC chips) on top of each other in achieving high-speed data transfer in computer servers.

As a single PIC may contain thousands of Si-photonic (optical) components, there is a need of developing design automation techniques similar to that for VLSI chips to produce PICs with better performance at lower cost and higher yield. Computer-aided-design (CAD) for Si-photonics has been explored for design of all-optical logic circuits [5] and for synthesis of combinational logic circuits [6]–[8]. Such optical circuits have been realized using different technologies such as electro-optic MZIs [9], ring resonators [10], photonic crystal gates [11], reversible logic gates [12], thermo-optic switches [13], terahertz optical asymmetric demultiplexer (TOAD) based interferometer switches [14] and so on. However, among these semiconductor optical amplifier (SOA) based Mach-Zender interferometer (MZI) is the cross-phase modulator, which acts as an optical switch and has been used as a building block in all-optical circuit design [15]. In all-optical circuit design, SOA-MZI switches are being used because of its advantages such as high-nonlinearity, high-speed, low switching energy, simplicity, compactness, stability and all-optical integration compatibility [15], [16]. Hence, SOA-MZIs have been used to design various all-optical circuits such as adders [17], [18], subtractors [19], multiplexers [20], counters [21], multipliers [22], etc. Multiplier is an important computational block used in on-chip-communication for frequency multiplications, in optical neural network architectures for high-performance computing for matrix multiplications, etc. Although, two-bit electro-optic multiplier [9] and programmable logic device (PLD) multiplier [22] have been reported in literature, it is hard to generalize the electro-optic multiplier [9] for n-bits, whereas PLD multiplier design [22] shows an exponential growth of optical cost with a higher precision bits.

In this paper, we present four different designs of all-optical multipliers, namely all-optical array multiplier (*Design1* and *Design2*) and all-optical CSA multiplier (*Design1* and *Design2*) using SOA-based MZIs and two design styles such as *Design1* (based on [18]) and *Design2* (based on [8]). Simulation results confirm that MZI-based CSA multiplier (*Design1*) has the lowest optical cost and delay compared to those of other three multiplier designs (CSA multiplier - *Design2*, array multiplier - *Design1*, array multiplier - *Design2*) with a precision of 2 or more bits. It is also evident from the simulation results that the proposed all-optical CSA multipliers are efficient in terms of optical cost and delay

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compared to PLD based multipliers [22] with a precision of 8 or more bits.

The remainder of the paper is organized as follows. Basic preliminaries and prior work are provided in Sec. II. Motivation and problem statement are presented in Sec. III. The proposed all-optical multiplier designs and their analysis are explained in Sec. IV and Sec. V, respectively. Comparative performance evaluation is presented in Sec. VI. Finally, the paper is concluded in Sec. VII.

II. Basic Preliminaries and Prior Work

In this section, we discuss about the basic preliminaries of designing photonic integrated circuits (PICs) and the related prior work reported in literature.

A. Silicon-Photonic (Optical) Components

In this subsection, we provide descriptions of three basic Si-photonic components used in an optical multiplier design. (1) **Beam Splitter (BS)** and **Beam Combiner (BC)**: Two passive optical components used to split a single light beam into and to combine n optical beams within the waveguides are denoted as $(1:n)$ BS and $(n:1)$ BC, respectively [23]. (2) **Coupler**: An optical coupler is used to provide the electrical isolation between input(s) and output(s). Fig. 1 shows two directional couplers (C_1 and C_2) consisting of two optical waveguides placed near to each other at some distance, whose output depends on the coupling coefficient [23].

(3) **Mach-Zender Interferometer (MZI)**: It is an amplitude modulator that consists of BSs and mirrors. The detailed working principle of MZI design has been explained in [23]. Another type of MZI is semiconductor optical amplifier (SOA) based MZI [24], which is one of the basic optical components used as an all-optical switch. A 2×2 optical switch based on SOA-MZI is shown in Fig. 1, where C_1 and C_2 are two couplers, and SOA_1 and SOA_2 are two SOAs. The control signal A and the input signal B are directed to port P_1 and P_2, respectively. Whereas, the output signals at two ports P_3 and P_4 depend on the control signal A. If control signal is present at port P_2, i.e., $A = 1$, then we get light at P_3, i.e., bar state (AB), while the absence of control signal, i.e., $A = 0$ generates an output at P_4, i.e., cross state ($\overline{A}B$).

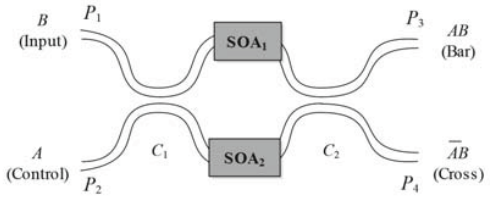

Fig. 1. Semiconductor optical amplifier (SOA) based MZI.

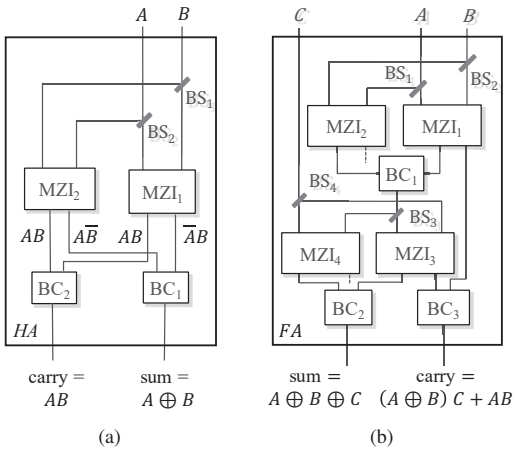

Fig. 2. MZI-based (a) half-adder and (b) full-adder based on design style in [18] (*Design1*).

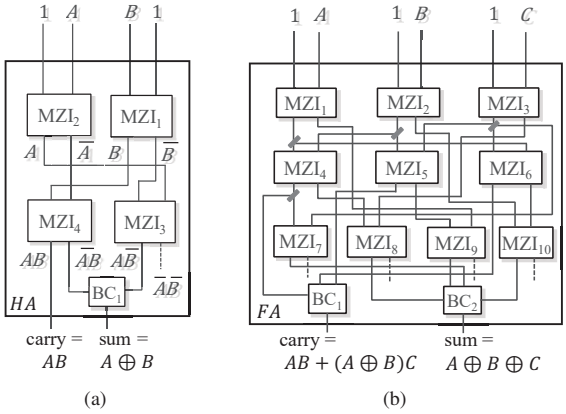

Fig. 3. Alternate design of MZI-based (a) half-adder and (b) full-adder based on design style in [8] (*Design2*)

B. Optical Circuit Design Parameters

The optical components are used to design an optical circuit, in which some components are provided with ancilla inputs (AIs), i.e., the extra input lines are required to add to maintain one-to-one mapping between inputs and outputs. The optical circuit may also generate garbage outputs (GOs) along with the final output(s), where GOs are neither the primarily output lines nor the input lines used by any other module. The seven design parameters for an optical circuit design are (1) N_{BS}, the total number of BSs, (2) N_{BC}, the total number of BCs, (3) N_{MZI}, the total number of MZIs, (4) N_{AI}, the total number of AIs, (5) N_{GO}, the total number of GOs, (6) Optical Cost, the total number of optical components used, i.e., sum of the number of BSs, BCs and MZIs used, and (7) Delay (Δ), the total number of MZIs used in the critical path of the design.

C. MZI-based Combinational Circuit Design

Half-adder and full-adder are the primitive modules to implement a multiplier. In this subsection, we discuss two

different design styles of SOA-MZI based half-adder and full-adder.

(1) **MZI-based Half-Adder (HA)**: In [18], a reversible optical HA has been designed, where sum and carry outputs are generated using 0 AI, 0 GO, 2 BSs, 2 BCs and 2 MZIs, as shown in Fig. 2(a). Since MZIs are connected in parallel, therefore the resultant delay of this design is equal to one unit. Similarly, another optical HA can be designed by binary decision diagram (BDD)-based synthesis technique as discussed in [8], which compromises of 2 AIs, 1 GOs, 0 BSs, 1 BCs and 4 MZIs with a delay of 2 units, as shown in Fig. 3(a).

(2) **MZI-based Full-Adder (FA)**: In [18], an optical full-adder (FA) has been designed using 0 AI, 2 GOs, 4 BSs, 3 BCs and 4 MZIs, as shown in Fig. 2(b). The critical path of this adder has 2 MZIs, therefore this FA design has a delay of 2 units. Similarly, another optical FA can be designed according to [8] using 3 AIs, 4 GOs, 4 BSs, 2 BCs and 10 MZIs with a delay of 3 units, as shown in Fig. 3(b).

D. Prior Work

In literature, all-optical reversible gates like Feynman [12] and Toffoli [12], all-optical digital logic gates like XOR [15], [16], AND [25] have been designed using SOA-MZIs. Some of the research work have presented logic circuit synthesis for bigger integrated optical circuits [6], [7]. Condrat *et al.* [6] presented design and synthesis of digital logic circuits using MZI switches, where XOR-based expression sharing has used to reduce the number of gates by using splitters at a cost of degraded signal strength. In [26], a splitter-free logic synthesis technique has been presented that can resolve signal degradation problem with an overhead of increased number of MZI switches.

In addition to this, researchers have also designed some optical and reversible combinational circuits [14], [19], [22], [27], [28]. All-optical reversible binary adder [5], reversible carry-lookahead adder [17], reversible carry-skip adder [18], binary full-adder [5], ripple carry adder and faster carry propagation adder [27] have been designed by using SOA-MZI as optical component. In [19], all-optical half-adder and full-adder designs have been proposed by using electro-optic MZIs. Gayen *et al.* [14] used TOAD-based tree architecture to design a basic all-optical arithmetic and logic unit (ALU) that can perform addition, subtraction, multiplexing, increment and decrement operations. In [20], n-bit all-optical reversible multiplexer design has been represented. Kumar *et al.* [29] presented all-optical half-adder and NAND logic using micro-ring structures. All-optical two bit multiplication has been presented using SOA-MZI based programmable logic device (PLD) [22], which can be generalized for higher or n-bit numbers. However, the generalization shows that there will be an exponential increase in optical cost. In [9], electro-optic MZIs have been used to design two bit multiplier which is not easy to cascade for n-bit multiplier. All-optical multiplication has been proposed using Sagnac switches [28], which is based on TOAD-based scheme. TOAD switches are loop mirror structure having SOA as non-linear element that have high switching speed. However, MZI-based switches have thermal stability, high signal-noise ratio, better bit-error rate and high data rates [16]. Therefore, in CAD for photonic circuit synthesis, SOA-MZIs have been extensively used as a basic optical component.

$A=(A_3A_2A_1A_0)$ $B=(B_3B_2B_1B_0)$				B_3	B_2	B_1	B_0	Multiplicand
				A_3	A_2	A_1	A_0	Multiplier
				B_3A_0	B_2A_0	B_1A_0	B_0A_0	$\Rightarrow PP_0$
			B_3A_1	B_2A_1	B_1A_1	B_0A_1	-	$\Rightarrow PP_1$
		B_3A_2	B_2A_2	B_1A_2	B_0A_2	-	-	$\Rightarrow PP_2$
	B_3A_3	B_2A_3	B_1A_3	B_0A_3	-	-	-	$\Rightarrow PP_3$
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	$\Rightarrow$ Final Product

Fig. 4. Multiplication of two 4-bit binary numbers A and B to obtain binary product A $\times$ B.

Among different arithmetic and logic units like adders, subtractors, multipliers, dividers, etc., few work have been found in literature on all-optical multiplier design. No work is reported on SOA-MZI based all-optical multiplier design with easy cascading for n-bit multiplication. Therefore, in this paper, all-optical n-bit multiplier has been presented using SOA-MZIs.

III. Motivation and Problem Statement

This paper presents two different design approaches for all-optical $n \times n$ multipliers using MZI-based optical switches.

A. Motivation

In literature, several research work have been reported for the design of all-optical adders, multiplexers, decoders. In order to realize an all-optical computational unit we also need to have the design of all-optical multiplier. Hence, we explore $n \times n$ multiplier designs using MZI-based optical switches (MZIs), where two n-bit binary numbers are taken as inputs. In future, these multiplier designs can be used by high-speed and high-precision optical computers.

In previous work, N_{AI}, N_{GO}, optical cost and Δ were considered as the design parameters for optimization in past. The optical cost was considered to be the total number of MZIs used in the circuit, while assuming the cost of BSs and BCs as zero. However, practically, the presence of any optical component in a logic circuit design affects its optical cost. Therefore, the numbers of BSs and BCs should also be included while calculating the total optical cost of the circuit.

B. Problem Statement

Two n-bit binary numbers A and B are taken as inputs, where A and B are multiplier and multiplicand, respectively. Our objective is to design all-optical multiplier to compute the product $A \times B$ with the help of MZI-based optical switches while calculating the design parameters N_{AI}, N_{GO}, N_{MZI}, N_{BC}, N_{BS} and Δ used in the design.

IV. Design of MZI-based All-Optical Multipliers

In this section, two different optical multiplier designs: array multiplier and CSA multiplier have been represented using BSs, BCs and MZIs. Both multipliers have been designed using two different design styles of SOA-MZI based HA and FA, named as *Design1* and *Design2*, where *Design1* follows the design style as discussed in [18] and *Design2* follows BDD-based technique [8].

The basic multiplication operation of two 4-bit binary numbers A and B is depicted in the Fig. 4 that has an 8-bit final product, i.e., $P_{[7:0]}$ as output. PP_i and B_jA_i are the partial product rows and partial product terms that will be provided as input to the optical array and optical CSA multiplier, respectively. The optical multiplier designs have been divided into two phases, where the first phase generates partial product terms and it is common in both designs while the second phase performs addition operations. Fig. 5 (a) represents the first phase of a 4-bit multiplier, where MZI bar state has been used to generate single product term. Therefore, the total number of MZIs required for this phase are equal to the number of B_jA_i terms, i.e., 16 MZIs. As all MZIs produce output in parallel, hence this phase has a total delay of 1 unit.

A. MZI-based Array Multiplier

Array Multiplier has a regular structure composite of optical HAs and FAs which are linked to each other in horizontal and vertical directions [30]. However, in this design, the execution speed is slow due to its large delay. The second phase of 4-bit array multiplier design has been presented in Fig. 5 (b), that takes B_jA_i as inputs and produce $P_{[7:0]}$ as final product. As in this design, total number of 4 HAs and 8 FAs have been used, therefore, all the parameters of array multiplier for second phase can be calculated as: (4 × HA + 8 × FA). Hence, *Design1* has a total number of 0 AI, 32 GOs, 48 BSs, 32 BCs and 56 MZIs with a delay of 21, whereas *Design2* uses a total number of 32 AIs, 52 GOs, 40 BSs, 20 BCs and 96 MZIs with a delay of 33. The designed optical array multiplier has large delay therefore, an another optical multiplier with lesser time delay has been designed.

B. MZI-based CSA Multiplier

MZI-based CSA multiplier is designed by linking CSAs in a tree like structure. CSA is a multi-operand adder that performs addition operation of three or more n-bit binary numbers and results partial sum (S_i) and partial carry (C_i) as two output sequences [30]. Given two n-bit numbers X and Y, S_i and C_i can be calculated as $S_i = X_i \oplus Y_i$ and $C_{i+1} = X_iY_i$, respectively. The second phase of MZI-based 4-bit CSA multiplier has been depicted in Fig. 6 (b), where four partial product terms of 6-bit each are provided as input to CSA blocks. A CSA block consists of a sequence of CSAs as shown in Fig. 6 (a), where all CSAs generate output in parallel. Finally, an optical ripple carry adder (RCA) [27] is used to generate the final product. Hence, 4-bit optical CSA multiplier *Design1* uses a total number of 0 AI, 74 GOs, 104 BSs, 72 BCs and 112 MZIs with an optical cost and delay of 288 and 19, respectively. *Design2* uses a total number of 144 AIs, 257 GOs, 209 BSs, 96 BCs and 547 MZIs with an optical cost and delay of 409 and 28, respectively. The design of 4-bit optical CSA multiplier shows a reduction in delay with an increased optical cost as compared to optical array multiplier design.

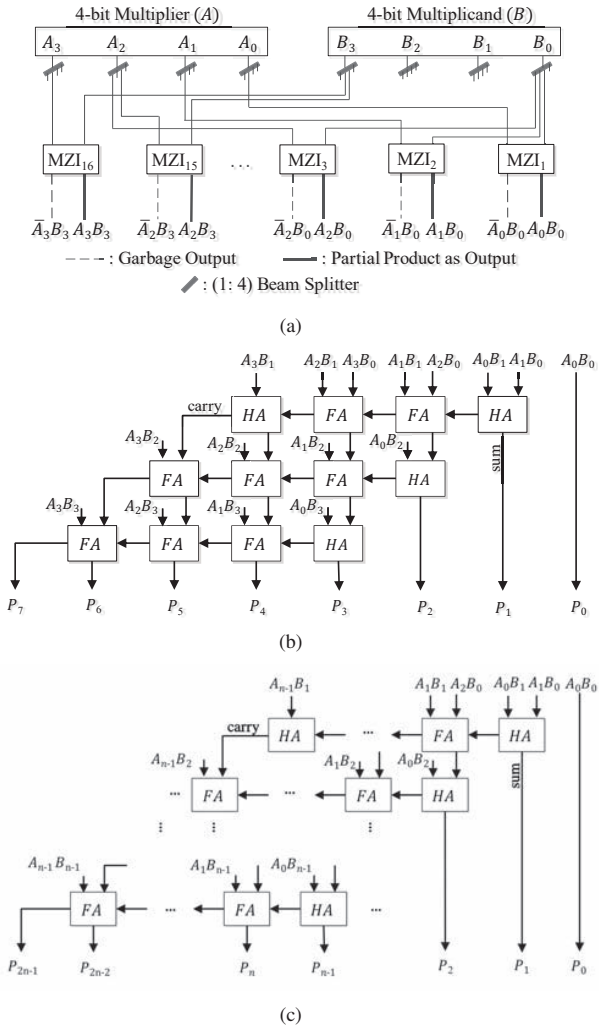

Fig. 5. MZI-based 4-bit array multiplier design: (a) Generating partial product terms and (b) obtaining final product. (c) MZI-based ***n***-bit array multiplier design.

V. Time and Space Complexities

The designed MZI-based array multiplier and CSA multiplier are divided into two phases: first phase (ϕ_1) and second phase (ϕ_2). The ϕ_1 includes the generation of partial product terms and ϕ_2 comprises the addition of the partial product terms that are output from the first phase. In this section, theoretical details about the optical design parameters in terms of space complexity (SC) and time complexity (TC) have been analyzed and discussed. The SC and TC for the

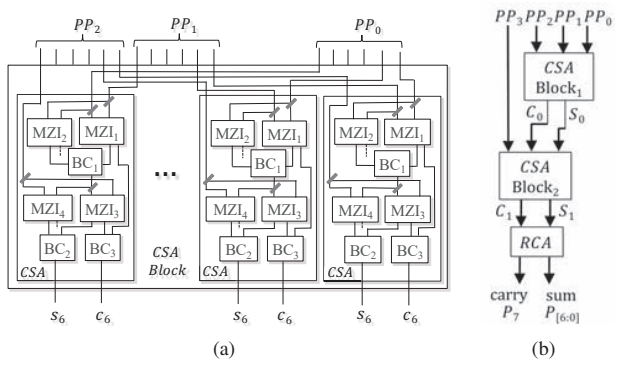

Fig. 6. (a) MZI-based 4-bit CSA block and (b) MZI-based 4-bit CSA multiplier design.

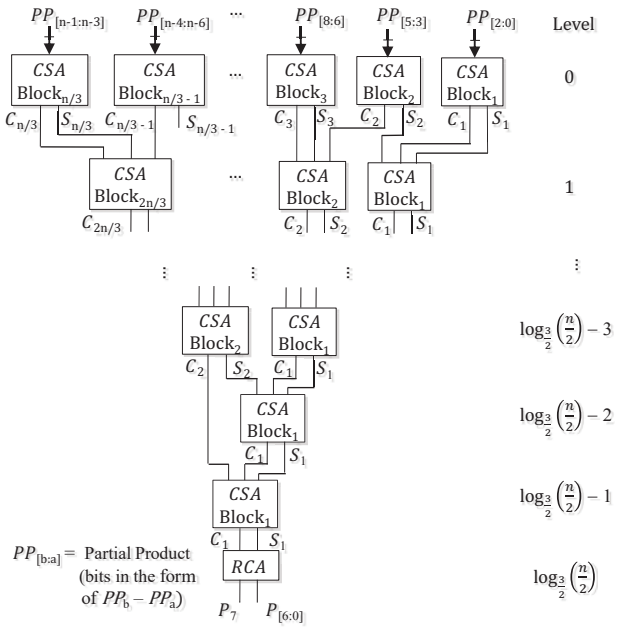

Fig. 7. MZI-based ***n***-bit CSA multiplier design.

complete design has been defined as $SC = SC(\phi_1) + SC(\phi_2)$ and $TC = TC(\phi_1) + TC(\phi_2)$, where $SC(\phi_i)$ and $TC(\phi_i)$ are the SC and TC for the ith phase.

Considering two n-bit binary numbers A and B as multiplier and multiplicand, respectively, as inputs to MZI-based multiplier. The ϕ_1 is common to both designs that requires n^2 number of product terms. Since, bar state of MZI generates product of two inputs, therefore, it can be used as an optical module for generating partial product terms. As one MZI module generates two outputs where one is the product term (bar state) and other is GO (cross state). Hence, a total of n^2 product terms can be generated with the help of n^2 number of MZIs that results a total of n^2 number of GOs. Each multiplicand and multiplier bit will be used n number of times by ϕ_1, therefore, $2n$ number of $1:n$ BSs are required by this module. All MZIs generate product terms in parallel, so ϕ_1 takes only a single unit Δ. Hence, the TC and SC for ϕ_1 can be presented as $TC(\phi_1) = \Delta = 1$ and $SC(\phi_1) = N_{BS} + N_{BC} + N_{MZI} = n^2 + 2n$, respectively. Further, $SC(\phi_2)$ and $TC(\phi_2)$ in MZI-based n-bit array and CSA multiplier designs have been described and compared.

A. MZI-based Array Multiplier

The second phase (ϕ_2) for $n \times n$ MZI-based array multiplier has been presented in Fig. 5 (c), that requires a total number of n and $n^2 - 2n$ HAs and FAs, respectively. The analysis has been calculated and discussed for both *Design1* and *Design2* as follows:

Design1: In *Design1* HA requires a total number of 2 MZIs, 2 BSs and 2 BCs with a delay of 1 unit, therefore the total optical cost is equal to the sum of MZIs, BSs and BCs, i.e, 6. Similarly, FA design has a delay of 2 unit and optical cost of 11 as it requires a total number of 4 MZIs, 4 BSs and 3 BCs. So, the optical cost for n and $(n^2 - 2n)$ HAs and FAs can be defined as $6n$ and $11(n^2 - 2n)$, respectively. This shows the $SC(\phi_2) = 6n + 11(n^2 - 2n) = 11n^2 - 16n$. Finally, SC for MZI-based array multiplier can be defined as: $SC = SC(\phi_1) + SC(\phi_2) = n^2 + 2n + 11n^2 - 16n = 12n^2 - 14n$. Now, the $TC(\phi_2)$ can be analyzed by calculating the Δ of the ϕ_2 design which is equal to the sum of the delay for n and $n^2 - 2n$ number of HAs and FAs, respectively. Therefore, time complexity for ϕ_2 can be calculated as: $TC(\phi_2) = n + 2(n^2 - 2n) = 2n^2 - 3n$. Finally, the TC for MZI-based array multiplier can be defined as: $TC = TC(\phi_1) + TC(\phi_2) = 1 + 2n^2 - 3n = 2n^2 - 3n + 1$.

Design2: The optical cost of HA and FA in *Design2* are 5 and 16 with a delay of 2 and 3, respectively. Now, the SC and TC can be analyzed in a similar way as it has been calculated for *Design1*. Similarly, the SC and TC for *Design2* can be defined as $17n^2 - 25n$ and $3n^2 - 4n + 1$, respectively.

B. MZI-based CSA Multiplier

MZI-based $n \times n$ CSA multiplier ϕ_2 has been depicted in the Fig. 7. It is a tree structure of CSA blocks and ripple carry adder (RCA) [27], where a single CSA block ($CSAb$) contains a sequences of CSAs. One CSA block can contain maximum of $2n$ number of CSA modules. Now, assuming the total number of CSA modules as N_{CSA}, levels as ℓ, CSA modules at level$_i$ as $N_{CSA}(\ell_i)$ and CSA blocks at level$_i$ as $N_{CSAb}(\ell_i)$ in ϕ_2 tree. The total $SC(\phi_2)$ can be analyzed as:

$$SC(\phi_2) = (N_{CSA} * SC(CSA)) + SC(RCA) \quad (1)$$

A $n \times n$ multiplier generates n number of partial product rows, therefore, $N_{CSAb}(\ell_0)$ are equal to $\frac{n}{3}$. Since, each CSA block produces two outputs, i.e., sum and carry. Hence, total number of outputs generated at ℓ_0 are $\frac{2n}{3}$, that will be input to ℓ_1. Now, $N_{CSAb}(\ell_1)$ will be equal to $\frac{2n}{3^2}$, which further produces $\frac{2^2 n}{3^2}$ number of outputs. Further, N_{CSAb} at each levels can be represented as: $\frac{2^\ell n}{3^{\ell+1}}$. Finally, the number of levels, i.e., ℓ can

TABLE I
COMPARATIVE RESULTS OF OPTICAL DESIGN PARAMETERS FOR MZI-BASED n-BIT MULTIPLIERS (WHERE "$Design1$" FOLLOWS DESIGN STYLE OF [18], "$Design2$" FOLLOWS DESIGN STYLE OF [8] AND "COST" MEANS "OPTICAL COST").

Parameters	PLD Multiplier [22]	MZI-based Array Multiplier		CSA Multiplier	
		Design1	*Design2*	*Design1*	*Design2*
N_{AI}	0	0	$3n^2-4n$	0	$6\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+6n$
N_{GO}	0	$3n^2-4n$	$5n^2-7n$	$n^2+2\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+8n$	$n^2+8\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+8n$
N_{BS}	0	$4n^2-4n$	$4n^2-6n$	$8\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+10n$	$8\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+10n$
N_{BC}	$2n-1$	$4n^2-6n$	$2n^2-3n$	$8\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+6n$	$4\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+4n$
N_{MZI}	$2^{2n}-1$	$5n^2-6n$	$11n^2-16n$	$n^2+8\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+8n$	$n^2+20\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+20n$
Cost	$2^{2n}+2n-2$	$12n^2-14n$	$17n^2-25n$	$n^2+22\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+24n$	$n^2+32\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+34n$
Δ	$2n$	$2n^2-3n+1$	$3n^2-4n+1$	$4n+2log_{\frac{3}{2}}\left(\frac{n}{2}\right)+1$	$6n+3log_{\frac{3}{2}}\left(\frac{n}{2}\right)+1$

be calculated as $\frac{2^{\ell+1}n}{3^{\ell+1}}=2$. Hence, total number of levels with CSA blocks are $\left\lceil log_{\frac{3}{2}}\left(\frac{n}{2}\right)\right\rceil$. Now, assuming the number of CSA modules in each CSA block as n_{cb} which is equal to $2n$, then N_{CSA} in the tree structure can be analyzed as follows:

$$N_{CSA}=N_{CSAb}*n_{cb} \tag{2}$$

where, N_{CSAb} represents the total number of CSA blocks present in design and it can be calculated as: $\frac{n}{3}+\frac{2n}{3^2}+\frac{2^2n}{3^3}+\cdots+\frac{2^\ell n}{3^{\ell+1}}=\left(\frac{2}{3}\right)^{\ell+1}n$, which is equal to $\left(\frac{2}{3}\right)^{\ell+1}n$. By substituting values of N_{CSAb} and n_{cb} in Equation 2, $N_{CSA}=2n^2\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}$. The SC of RCA module from [27] has been analyzed as: $SC(RCA)=N_{BS}(RCA)+N_{BC}(RCA)+N_{MZI}(RCA)$, where $N_{BS}(RCA)$, $N_{BC}(RCA)$ and $N_{MZI}(RCA)$ are the number of BSs, BCs and MZIs used in RCA design. Now, SC and TC for n-bit optical CSA multiplier *Design1* and *Design2* have been calculated as follows:

Design1: A CSA module in *Design1*, uses a total number of 4 BSs, 3 BCs and 4 MZIs which results space complexity of CSA ($SC(CSA)$) as 11. For $2n$-bit RCA, $SC(RCA)$ and $TC(RCA)$ w.r.t. *Design1* are analyzed as $22n$ and $4n$, respectively. Now, substituting values of N_{CSA}, $SC(CSA)$ and $SC(RCA)$ in Equation 1, the $SC(\phi_2)$ has been calculated as: $\left[2n^2\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}\right]*11+22n$. Finally, the SC of MZI-based CSA multiplier is analyzed as: $SC=SC(\phi_1)+SC(\phi_2)$ = $(n^2+2n)+11\left[2\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+22n$ = $n^2+22\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+24n$. Now, TC of ϕ_2 can be analyzed as: $TC(\phi_2)=2\ell+\Delta(RCA)$, which is equal to $2log_{\frac{3}{2}}\left(\frac{n}{2}\right)+4n$. Therefore, the total TC of the CSA multiplier design is defined as $TC=TC(\phi_1)+TC(\phi_2)$, is equal to $1+4n+2log_{\frac{3}{2}}\left(\frac{n}{2}\right)$.

Design2: A single CSA module in *Design2*, uses 4 BSs, 2 BCs and 10 MZIs which calculates $SC(CSA)$ as 16. The $SC(RCA)$ and $TC(RCA)$ for $2n$-bit RCA has been calculated as $32n$ and $6n$, respectively. Now, SC of MZI-based CSA multiplier for *Design2* can be calculated in a similar way as done in *Design1*, which is equal to $(n^2+2n)+16\left[2\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+32n = n^2+32\left[\left(\frac{2}{3}\right)^{log_{\frac{3}{2}}\left(\frac{n}{2}\right)}n^2\right]+34n$. Similarly, the TC has been calculated as $1+6n+3log_{\frac{3}{2}}\left(\frac{n}{2}\right)$. The comparative results of optical design parameters for both designs have been summarized in Table I, which shows that the MZI-based CSA multiplier is better in terms of TC and SC compared to array multiplier.

VI. PERFORMANCE EVALUATION

All multiplier designs have been implemented using the hardware description language Verilog, where optical module library of MZI, BS, BC, HA and FA have been implemented and used to designs all-optical multiplier. The simulation results of optical array and optical CSA multiplier (*Design1* and *Design2*) for varying input bits, have been shown in the Table II. As 2-bit optical CSA multiplier design is same as optical array multiplier design, therefore, the optical parameters for both multiplier designs are same. The simulation results shows that 8 or greater than 8-bit MZI-based CSA multiplier has lesser optical cost and delay as compared to array multiplier. 128-bit MZI-based CSA multiplier – *Design1*, reduces the optical cost and delay by 9.4 and 60.87 times while optical CSA multiplier – *Design2*, reduces the optical cost and delay by 8.8 and 60.80 times as compared to 128-bit MZI-based array multiplier – *Design1*. Similarly, the simulation

TABLE II
COMPARATIVE RESULTS FOR DIFFERENT MZI-BASED MULTIPLIERS WITH VARYING NUMBER OF BITS (WHERE "$Design1$" FOLLOWS DESIGN STYLE OF [18], "$Design2$" FOLLOWS DESIGN STYLE OF [8] AND "COST" MEANS "OPTICAL COST").

	MZI-based array multiplier – *Design1*							**MZI-based CSA multiplier – *Design1***						
n (**#Bits**)	N_{AI}	N_{GO}	N_{BS}	N_{BC}	N_{MZI}	**Cost**	Δ	N_{AI}	N_{GO}	N_{BS}	N_{BC}	N_{MZI}	**Cost**	Δ
2	0	4	8	4	8	20	3	0	4	8	4	8	20	3
4	0	32	48	32	56	136	21	0	74	104	72	112	288	19
8	0	160	224	160	272	656	105	0	160	209	144	257	611	38
16	0	704	960	704	1184	2848	465	0	449	419	290	643	1354	74
32	0	2944	3968	2944	4928	11840	1953	0	1412	841	583	1801	3226	143
64	0	12032	16128	12032	20096	48256	8001	0	4876	1688	1170	5656	8515	273
128	0	48640	65024	48640	81152	194816	32385	0	17949	3386	2347	19514	25249	532
	MZI-based array multiplier – *Design2*							**MZI-based CSA multiplier – *Design2***						
n (**#Bits**)	N_{AI}	N_{GO}	N_{BS}	N_{BC}	N_{MZI}	**Cost**	Δ	N_{AI}	N_{GO}	N_{BS}	N_{BC}	N_{MZI}	**Cost**	Δ
2	4	6	4	2	12	18	5	4	6	4	2	12	18	5
4	32	52	40	20	112	172	33	72	112	104	48	256	409	28
8	160	264	208	104	576	888	161	144	257	209	96	547	852	58
16	704	1108	928	464	2560	3952	705	290	643	419	193	1225	1838	112
32	2044	4896	3904	1952	10752	16608	2945	583	1801	841	388	2968	4198	211
64	12032	20032	16000	8000	44032	68032	12033	1170	5656	1688	780	7996	10465	409
128	48640	81024	64768	32384	178176	275328	48641	2347	19514	3386	1565	24210	29162	799

results shows that the optical multiplier *Design1*, has lesser optical cost and delay compared to *Design2*.

In previous work, 2-bit multiplier designs based on electro-optic MZI [9] and SOA-MZI based PLD [22] have been proposed. In this section, the optical design parameters of MZI-based array and MZI-based CSA multiplier designs have been compared with the exiting work. In [9], 2-bit multiplier design uses 14 N_{MZI}, 10 N_{GO} with a delay (Δ) of 5 units. Therefore, the comparative results of 2-bit MZI-based array and CSA multiplier designs from Table II, show a total improvement of 42.85%, 60% and 40% in terms of N_{MZI}, N_{GO} and Δ, respectively with respect to *Design1*. The 2-bit multiplier with respect to *Design2*, shows a total improvement of 14.28% and 40% in terms of N_{MZI} and N_{GO} with a similar Δ. In addition, [9] design uses a total number of 4 electro-optic converters that further affects the design cost and delay. Similarly, 2-bit multiplier designs has been compared with all-optical PLD multiplier design [22]. The design from [22], uses 15 N_{MZI}, 0 GO with a Δ of 4 unit. Hence, *Design1* shows a total improvement of 20% and 25% in terms of N_{MZI} and Δ, respectively, with an overhead of increased N_{GO}. Similarly, the 2-bit multiplier in respect of *Design2*, shows a improvement of 20% in N_{MZI} with an increase of 25% in Δ, respectively.

Further, in this work, PLD multiplier [22] design has been generalized for n-bit and the calculated optical design parameters have been presented in Table I. Fig. 8 (a) and (c) shows the graphical comparison of MZI-based array, CSA and PLD multiplier designs in terms of delay (Δ) and optical cost, respectively with varying number of input bits. Fig. 8 (c) depicts that the PLD multiplier [22] has least delay compared to other multiplier designs. However, the optical cost of PLD multiplier increases exponentially with the number of input bits, as shown in Fig. 8 (b). Therefore, PLD multiplier [22] design performs better in terms of both cost and delay for smaller number of input bits (till 8-bits). However, for the higher number of bits, e.g., 128-bit PLD multiplier [22] shows an approximate 190 and 3 times less delay with respect to array and CSA multiplier designs with an approximate increase of 10^{34} times in terms of optical cost compared to other designs. Therefore, the comparative results show that PLD multiplier [22] design can be used for smaller bits, however, this design can not be extended and used for higher speed precision computers.

Fig. 8 (c), represents the closer view of the Fig. 8 (b) for array and CSA multiplier optical cost comparison. Fig. 8 (c) shows that 4-bit CSA multiplier has higher optical cost compared to array multiplier, while for higher input bits (greater than 4), all CSA multiplier designs outperform in terms of cost and delay compared to array multiplier designs.

VII. CONCLUSIONS AND FUTURE WORK

In recent years, design of all-optical computational units has received attention from the CAD researchers. In this paper, two different designs of all-optical multipliers have been presented. The performance evaluation of optical parameters shows that all-optical CSA multipliers perform better in terms of both optical cost and delay compared to those of all-optical array multipliers. A complete analysis of different designs of computer arithmetic blocks can be performed as a future work to study the trade-off between time and space complexities. The current optical multiplier design can be optimized further while reducing the number of garbage output lines and reducing the number of beam splitters along all the paths from input to output for better signal strength.

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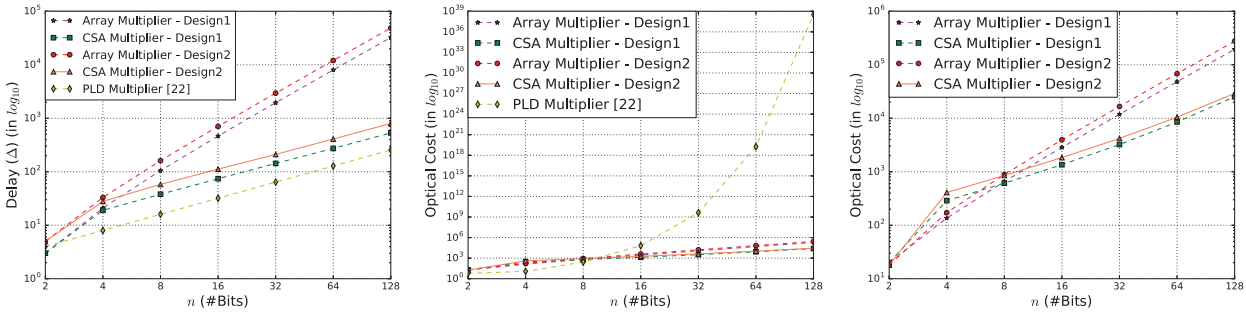

Fig. 8. Variation of (a) delay (in log_{10} scale), (b) optical cost (in log_{10} scale), and (c) closer look of optical cost (in log_{10} scale) with increasing number of bits (n).

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