Design of a radiation-tolerant high-speed driver for Mach Zender Modulators in High Energy Physics

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Abstract—This paper presents the integrated circuit design, targeting a CMOS 65 nm 1.2 V technology, of a high-speed driver that provides the differential input signals to a Mach Zender Modulator (MZM), and allows tuning of the MZM operating point through adjustment of the bias voltage. A multi-voltage domain circuit is proposed, where each domain is isolated through deep n-well trenches, to face the high voltage swing and the bias regulation requirements of the MZM. The MZM device, whose prototype has been implemented in silicon photonics iSiPP50G technology, is emerging as a promising solution for radiation tolerant, several hundreds of Mrad, and high-speed, in the range of 10 Gbps, optical links. These stringent requirements are needed in high energy physics experiments in the upgrade of the Large Hadron Collider or in future Linear Colliders.

Keywords: High-speed CMOS driver, Mach-Zender Modulator driving circuit, Radiation tolerance, High energy physics

I. INTRODUCTION

The increase of the luminosity in future accelerators for High Energy Physics (HEP) experiments will require the complete re-design of the Front-End (FE) electronics to face high data rates in the Large Hadron Collider [1], after the high luminosity upgrade scheduled in 2025, and in linear colliders, such as the CLIC (Compact Linear Collider), foreseen at CERN. There will be new harsh requirements for the FE electronics in terms of data rates and radiation tolerance: up to 5 Gbps from each FE ASIC and a Total Ionizing Dose (TID) up to 1 Grad in the inner layers of the Silicon Trackers.

Radiation tolerant (~1 Grad) high-speed (~10 Gbps) optical links will be required for data acquisition and distribution of Timing, Trigger and Control (TTC) signals [2]. Optical links based on Mach Zender Modulator (MZM) devices, apart their use in consumer/telecom applications [3, 4], are emerging as a possible alternative to standard links based on Light Emitter Diode (LED) and Vertical Cavity Surface Emitting Laser (VCSEL) devices [5-7]. The MZM is based on the principle of the MZ interferometer where an input optical continuous wave (CW) is splitted in two branches, each with its own phase shifter. In our project an optical CW with a wavelength of 1550 nm (transparent to silicon) is produced by a SiGe Photodiode. Thanks to interference with a differential RF signal propagating in an electrical waveguide, the optical properties of the MZ interferometer are changed in a different way between the two branches, i.e. in the two optical phase shifters. The two optical signals are then recombined at the output of the MZ interferometer resulting in an optical wave modulated by the RF signal, see Fig. 1.

To address the development and the characterization of a demonstrator of a 1 Grad 10 Gbps radiation-tolerant optical link based on MZM the PHOS4BRAIN project has been started as a collaboration between INFN-Pisa, University of Pisa, CERN and SSSUP. A key building block of the demonstrator is the MZM Driver (MZMD), an integrated circuit designed in TSMC CMOS 65nm technology that provides the differential input signals to the MZM and allows tuning of the MZM operating point through adjustment of the bias voltage. After the introduction, this work in Section II discusses the specification of the integrated driver for a MZM, which has been implemented by the CERN partner in IMEC *ePIXfab SiPhotonics* iSiPP50G technology [7]. Section III deals with the driver circuit architecture, with a focus on its main sub-blocks. Section IV presents the transistor-level simulation performance results when the circuits are implemented in the TSMC 65 nm CMOS 1.2 V technology. Conclusions and future works are drawn in Section VI.

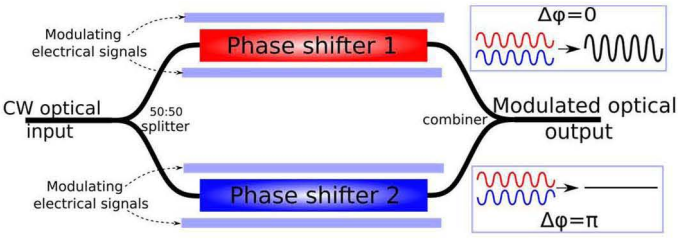

Fig. 1: Architecture of a MZM

II. MZM DRIVER SPECIFICATIONS

A simple equivalent circuit of a MZM driven by the MZMD circuit is shown in Fig. 2. As a first order approximation, each RF input (Sig+ and Sig-) of the MZM has an equivalent input impedance that can be modeled as a diode with a 50 Ω termination in parallel. The required bias voltage to properly polarize the MZM diodes should be 2 V and should be adjustable in order to optimize the device performance with respect to environmental conditions (temperature, aging, radiation damage). The peak-to-peak difference between the input signals Sig+ and Sig- should be 2V. Although thick-oxide transistors are available in the 65 nm CMOS technology, and they could provide output voltages up to 3.3V, as in [8], they can not be used since they cannot guarantee the required radiation tolerance. Indeed, as proved in literature, thick-oxide devices are very sensitive to TID effects [9]. On the other hand, thin-oxide devices in 65 nm CMOS technology can not stand voltages higher than 1.2 V. To overcome this issue, in the proposed design, see Figs. 2 and 3, we introduced electrically insulated voltage domains, by using deep n-wells. The three different boxes in Figs. 2 and 3 represent the 3 different voltage

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domains in the MZM driver circuit (deep N-well allows to insulate P-doped regions containing the different voltage domains from the P-doped substrate):

- Blue box: Lower Voltage Domain [-VDD, GND] in the p-doped substrate.
- Light Blue box: Intermediate Voltage Domain [-VDD/2, +VDD/2] in a first p-doped region insulated from the substrate.
- Red box: Higher Voltage Domain [GND, +VDD] in a second p-doped region insulated from the substrate.

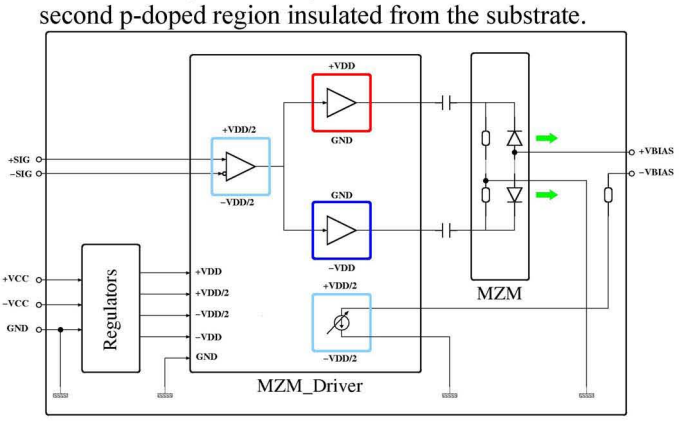

Fig. 2: MZM circuit architecture

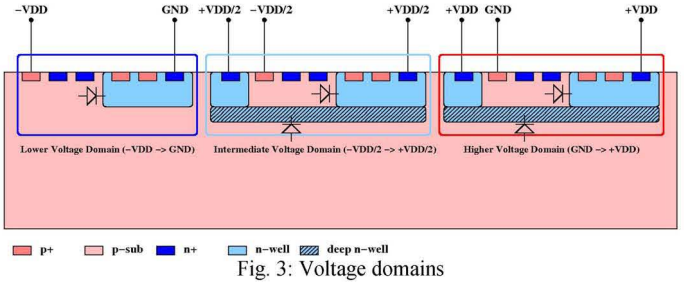

Fig. 3: Voltage domains

III. MZM Driver Architecture

The detailed architecture of the MZM driver circuit is shown in Fig. 4. Main building blocks are:

- Differential Output Driver (OD) => it provides the Sig+ and Sig- signals to the two MZM branches.
- Level Translator (LT) => it interfaces the different voltage domains.
- 20-bit Serializer (SER) => when it is enabled, it provides input data stream to the Differential Output Driver.
- SLVS Differential Receiver (RX) => it converts to CMOS levels the SLVS (Scalable Low Voltage Signaling) levels of the differential input used as clock of the serializer or as input of the Differential Output Driver. An architecture based on a chain of inverting buffers has been used to implement the SLVS RX.
- Timing Adjustment (TA) Module => It allows the phase alignment between Sig+ and Sig-.
- Bias Adjustment (BA) module => it allows adjustment if the MZM bias voltage through fine tuning of bias current.

An SPI Interface is used to provide an access to control and status registers. Hereafter, we detail the main sub-blocks.

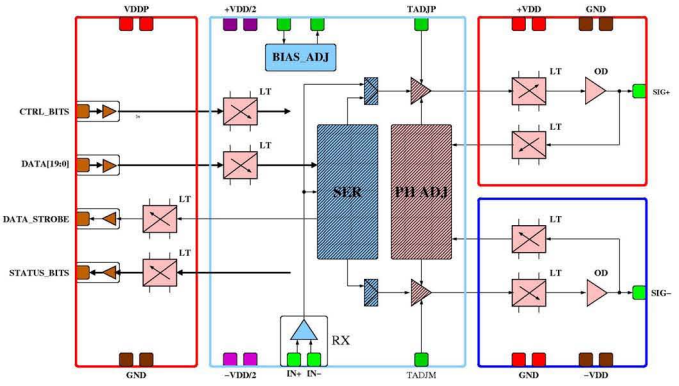

Fig. 4: Architecture of the MZM driver

A. Output Driver

The two output drivers, one for the [–VDD, GND] domain (blue in Fig. 5) and the other for the [GND, +VDD] domain (red in Fig. 5), have to drive the MZM with rail-to-rail signals. This is done using a voltage driving method, with low-resistance connections allowing the required voltage levels. Each driver is driven by two differential signals, which are generated in the [-VDD/2, VDD/2] domain and translated in the other two domains. Before the "final stage" some buffers are used to increase the driving capability of the differential pair amplifier (architecture in Fig. 5 and transistor-level schematic in Fig. 6).

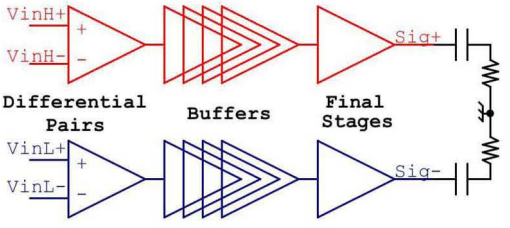

Fig. 5 Architecture and of the Output Driver

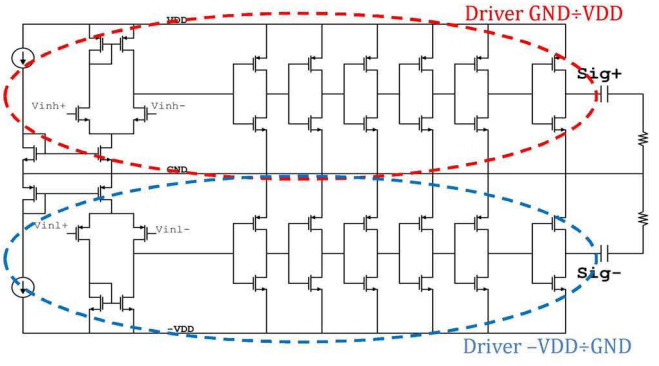

Fig. 6: Transistor-level scematic of the Output Driver

B. Level Translator

This block is widely used inside the chip to ensure the communication between blocks in different voltage domains. The "up" or "down" translator is placed between two voltage domains and it is made from two blocks, one placed in the source-domain and the other in the sink-domain. In Figs. 7 and 8 the two blocks of an up-translator are shown, architecture Fig. 7 and transistor-level circuit in Fig. 8. It translates the

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signals from the [–VDD/2, +VDD/2] domain to the [GND, +VDD] domain using the common range [GND, +VDD/2] as interface. The down-translator uses the same principle.

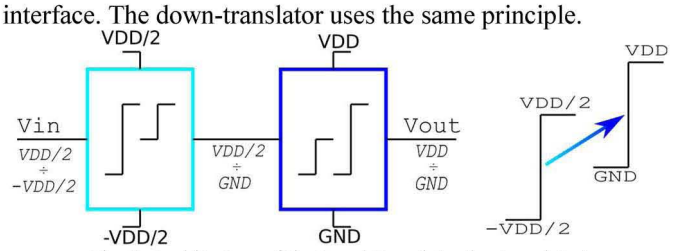

Fig. 7: Architecture of the Level Translator (up-translator)

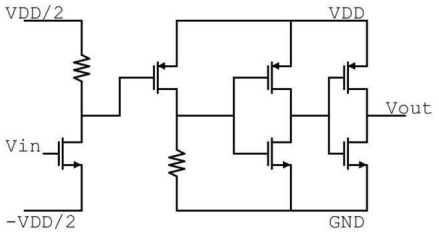

Fig. 8: Circuit schematic of the Level Translator (up-translator)

C. 20-bit Serializer

The SER architecture in Fig. 9 is derived from the architecture of the CHIPIX65 2 Gbps Serializer [10]. Three 20-bit shift registers (LG_SHR) generate (every 20 clock cycles):

i) the command used to load the parallel input data into other three 20-bit shift registers (SHR);
ii) set and reset commands used to generate the data strobe SER output that can be used as a read clock for and external data source (e.g. FIFO).

Triple Modular Redundancy (TMR) is used to correct, in the Majority Logic (ML) units, Single Event Effects (SEE)-induced errors in the LG_SHR and SHR shift registers, similarly to what we proposed in [11]. Standard Cells had been used in the CHIPIX65 Serializer because of the relatively low required speed. Instead, in the MZM driver, standard cells have been replaced by custom faster dynamic cells with MOS devices "wide" enough (> 4x minimum size) to get the required tolerance vs. TID effects.

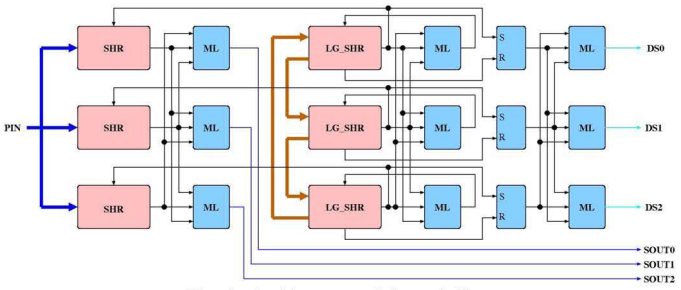

Fig. 9: Architecture of the serializer

D. Timing Adjustment Module

The two drivers are in two separate voltage domains, see Figs. 2 and 4; so between the generated signals there could be a phase shift, which affects the performance of the MZM. To avoid this effect a feedback control has been implemented to guarantee the correct phase alignment. The Phase Adjustment block takes the two output signals, translates them thanks to level translators and compares them. After the comparison, the control signals are filtered and used to delay a line and to speed up the other. The phase of the signals in the drivers is shifted using starved-NOTs, which use controlled currents to change rise and fall times of the output signals, see Fig. 10.

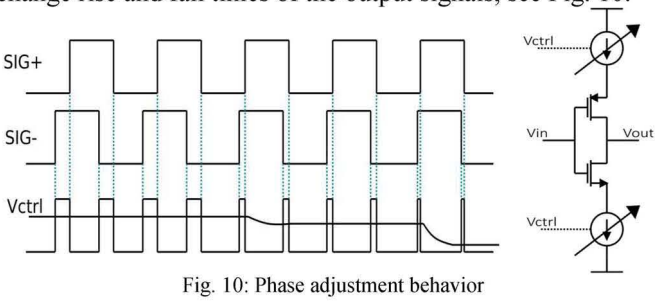

Fig. 10: Phase adjustment behavior

E. Bias Adjustment Module

The diodes of the MZM to be properly polarized need an adjustable bias voltage of 2 V ± 0.5 V. This voltage is higher than the maximum voltage manageable in this technology so an external generator is used for the 2 V generation, delegating the adjustable part inside the chip. As shown in Fig. 2, the working principle is based on the control of the reference voltage of the external generator, using a resistance and a controlled current generator. Fig. 11 shows the transistor level schematic of the current generator, which is controlled by a 6-bit register (MSB 'b5' controls the current direction and the other bits its value).

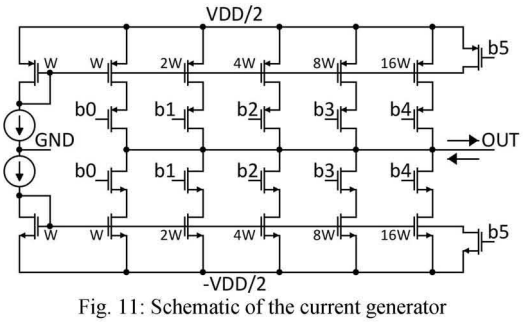

Fig. 11: Schematic of the current generator

IV. MZM Driver Performance

The circuit solutions proposed in Section III have been implemented in a TSMC 65 nm CMOS technology, for which TID and SEE radiation–damage models are available, since this technology has been already used for radiation-hardened design in CERN HEP experiments. By using these models, we estimate that the proposed circuit is able to reach a data rate of 10 Gbps in non-irradiated conditions (see transistor level simulation results in Cadence Spectre environment in Figs. 12 to 15) and a data rate of at least 5 Gbps, after 0.5 Grad radiation-damage. Fig. 12 shows simulation results of the two drivers in Fig. 6. The SIG+ and SIG- are the output signals of the two drivers, while the OUTH and OUTL are the signals taken after the DC decoupling capacitors. The bit-rate of this simulation confirms the suitability of the design for 10 Gbps. Fig. 13 shows simulation results of the level translator in Fig. 8, still at 10 Gbps. The green line is the input signal, in the intermediate domain [-VDD/2, VDD/2]. This signal is traslated in the common range [GND, VDD/2] (blue line) and

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then in the higher domain [GND, VDD] (red line). The current budget for the MZM driver is 80 mA overall, of which 60 mA in the differential output driver block. Fig. 14 shows simulation results for a 10-bit scaled version of the Serializer. A constant data (0x32C) is loaded in the data shift register (SHR) when the LOAD signal is high. Data propagation in the LG_SHR and SHR shift registers is shown. Fig. 15 shows simulation results at 10 Gbps for the SLVS receiver, with SLVS differential inputs (Vin), voltages in the intermediate nodes (Vint) and output voltages.

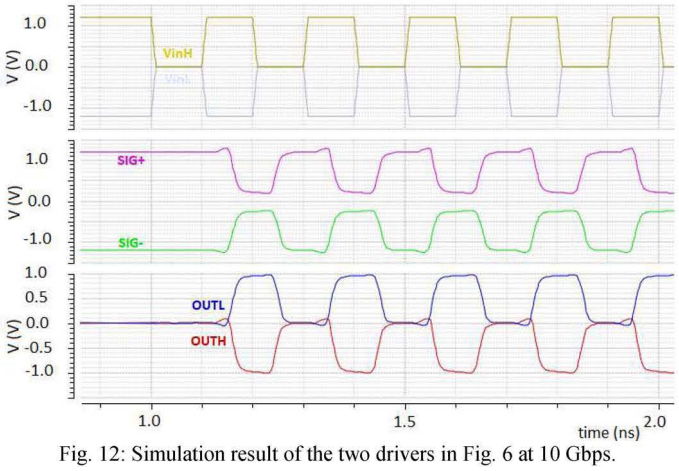

Fig. 12: Simulation result of the two drivers in Fig. 6 at 10 Gbps.

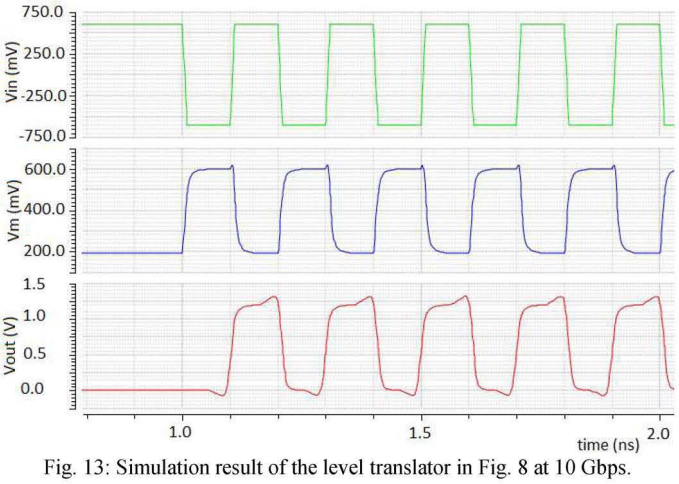

Fig. 13: Simulation result of the level translator in Fig. 8 at 10 Gbps.

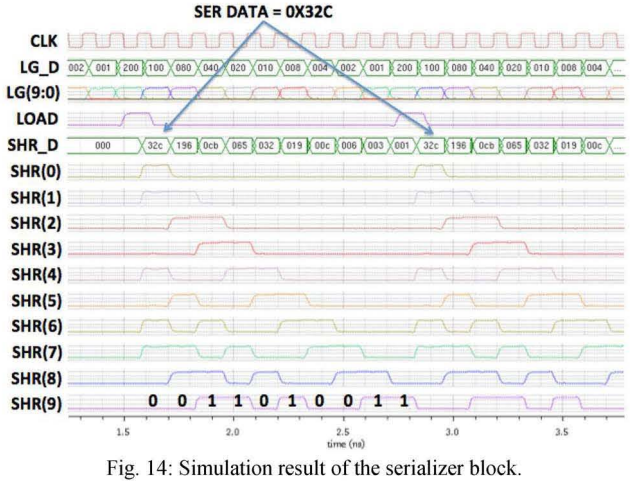

Fig. 14: Simulation result of the serializer block.

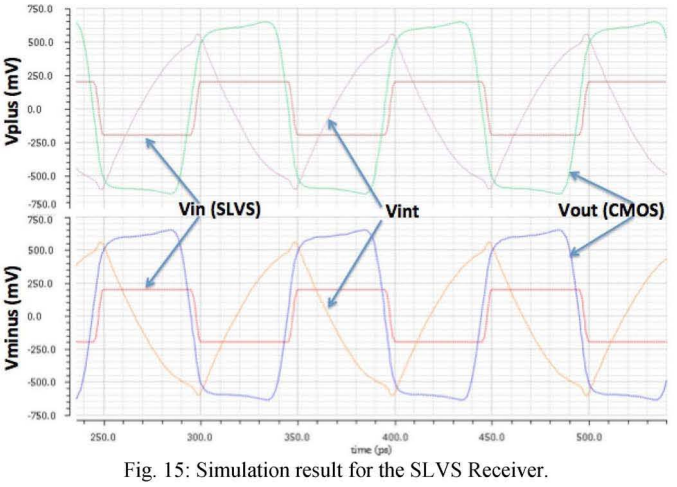

Fig. 15: Simulation result for the SLVS Receiver.

V. CONCLUSIONS AND FUTURE WORKS

This paper has presented the integrated circuit design of a 10 Gbps driver that provides the differential input signals to a Mach Zender Modulator (MZM), and allows tuning of the MZM operating point through adjustment of the bias voltage. The MZM device, whose prototype has been implemented in silicon photonics iSiPP50G technology, is emerging as a promising solution for radiation tolerant, in the range of 1 Grad, and high-speed, in the range of 10 Gbps, optical links. Targeting a CMOS 65 nm technology, as in [12], without using thick-oxide devices to avoid TID radiation damage problems, a multi-voltage domain circuit is proposed to face the high voltage swing and the bias regulation requirements of the MZM, 2 V vs. the max. 1.2 V of the technology. The multiple voltage domains are isolated through deep n-well trenches. Circuit solutions for the differential output driver, high-speed serializer, level translator, SLVS differential receiver, timing adjust module and bias adjust module are presented. Circuit-level simulation results prove the suitability of the proposed circuit to meet the stringent requirement of a 10 Gbps MZM driving capability. The current budget for the whole circuit is 80 mA, of which 60 mA are needed to ensure a fast swing of the differential output driver. A characterization of the proposed circuit design vs. TID and SEE effects is still on going. However, previous experience on circuits manufactured in the same technology, and using devices with similar size, allow us to estimate a radiation tolerance of several hundreds of Mrad. As future work, the circuit will be fabricated in the 65 nm 1.2V TSMC technology and tested together with the MZM already fabricated in the iSiPP50G technology, to measure the speed degradation after TID and SEE radiation damage. Differently from [3] temperature effect is a lower issue in HEP experiments since the chip will work at a nearly constant ambient temperature of -30 °C. The design of a current mode logic MZM driver is also planned to face a radiation-tolerance up to 1 Grad [13]. Beside high-energy physics, integrating driver and MZM for high-speed photonics links is useful also in ground and aerospace vehicles [14].

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REFERENCES

[1] S. Seif El Nasr-Storey, et. al., "Effects of Radiation on a Mach-Zehnder Interferometer Silicon Modulator for HL-LHC Data Transmission Applications", IEEE Transactions on Nuclear Science, 62 (1), 2015

[2] D. Underwood, B. Salvachua-Ferrando, R. Stanek, D. Lopez, J. Liu, J. Michel, L. C. Kimerling, "New optical technology for low mass intelligent trigger and readout," Journal of Instrumentation, 5 (7), 2010.

[3] S. Liu et al., "A temperature independent driver for Mach-Zehnder modulators", IEEE ISCAS 2015, pp. 1474-1477

[4] M. A. Seyedi et al., "Silicon Mach-Zehnder Interferometer modulator with PAM-4 data modulation at 64 Gb/s", IEEE MWSCAS2015

[5] D. Gajanana et al., "Irradiation Tests on InP-based Mach-Zehnder Modulator", Topical Workshop on Electr. for Particle Physics, 2012.

[6] M. Zeiler et al., "A system-level model for high-speed radiation-hard optical links in HEP experiments based on silicon Mach-Zehnder modulators", Journal of Instrumentation, 11 (C12059), 2016

[7] M. Zeiler et al, "Radiation Damage in Silicon Photonic Mach-Zehnder Modulators and Photodiodes", IEEE Transactions on Nuclear Science, 2017, 64 (11), 2017, pp. 2794 - 2801

[8] Ke Li et al. "A 30 Gb/s CMOS driver integrated with silicon photonics MZM", IEEE RFIC Symposium 2015, pp. 311-314

[9] S. Bonacini, P. Valerio, R. Avramidou, R. Ballabrifa, F. Faccio, K. Kloukinas, A. Marchioro, "Characterization of a commercial 65 nm CMOS technology for SLHC applications", Journal of Instrumentation 7 (P01015) 2012, pp. 1-14

[10] G. Magazzù et al., "Radiation tolerant serial links for high-speed data transfer in High Energy Physics experiments", Topical Workshop on Electr. for Particle Physics, 2017

[11] N. Costantino, G. Borgese, S. Saponara, L. Fanucci, J. Incandela, G. Magazzu, "Development, design and characterization of a novel protocol and interfaces for the control and readout of front-end electronics in high energy physics experiments", EEE Transactions on Nuclear Science, 60 (1), 2013, pp. 352-364

[12] N. Demaria et al., "Recent progress of RD53 collaboration towards next generation pixel read-out chip for HL-LHC", Journal of Instrumentation, 11 (12), 2016, C12058

[13] J. Butler et al, "Technical proposal for the phase-II upgrade of the CMS detector", CERN-LHCC-2015-010

[14] P. Reviriego et al., "Introducing energy efficiency in the VDE 0885-763 standard for high speed communication over plastic optical fibers", IEEE Communications Magazine, 51 (8), 2013, pp. 97-102