A Coupled Inductor Based Single Stage High Gain DC-AC Buck-Boost Inverter

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Abstract

Two stage conversion systems (TSCSs) normally use either boost converter or high gain dc-dc converter along with dc-ac inverter in order to transfer power from low input voltage dc source to high voltage ac load. When these TSCSs operate at extremely low input voltages, the boost converter has to operate at extremely high duty ratios. This in turn results in more losses and reverse recovery problems. Usage of high gain dc-dc converter results in more number of components, increase in control complexity and decrease in reliability. Single stage conversion systems (SSCSs) are formed by merging both dc-dc and dc-ac conversion processes. These SSCSs have advantages like low loss, more compact and less reverse recovery problems. In this paper, a high gain coupled inductor based single-phase SSCS is presented. This SSCS topology has many desirable features such as high gain, less switching losses, free from leakage inductance adverse effects and compact. Principle of operation, steady state analysis and design of the proposed topology are described in detail. MATLAB Simulation results of the proposed topology and experimental results using DSP28335 based experimental setup are presented to validate the proposed scheme.

Keywords: Single stage, high gain, dc-ac converter, coupled inductor, buck-boost inverter.

1 Introduction

Output voltage from photovoltaics (PV) is dc, which depends on several factors like insolation, temperature etc. This voltage varies all the time depending upon the aforementioned factors. To deliver power to loads or grid from PV, a suitable power conversion system (PCS) is required [1], [2], [3]. The PCS has to buck/boost the input voltage followed by dc-ac power conversion. This is a typical two stage power conversion system. Several two stage PCSs have been reviewed in [4], [5]. Two stage PCS is a cascade connection of high gain dc-dc buck/boost converter and dc-ac inverter. This kind of PCS suffers from several drawbacks like lower efficiency, lower reliability, large size and higher cost, especially when it operates at low input voltages [6]. Single-stage topologies combine the performance of each stage in multistage power converters, which in turn results in high efficiency, more reliability and low cost [7].

As SSCS gives several advantages compared to TSCS, research focus has shifted towards SSCS. A topology named boost inverter is proposed in [8], which is derived by connecting load differentially across two boost converters which are operating at 180 degrees out of phase. Though this topology has less component number, it suffers from high switching losses and EMI problems. Kasa et al., proposed a SSCS topology based on half-bridge buck-boost inverter configuration in [9]. This topology has minimum switching and conduction losses because only two devices are operated during any half cycle of output voltage. The drawback of this topology is improper utilization of PV source. Kasa et al., proposed another topology in [10], which works on buck-boost principle. This converter uses minimum number of switches (three), but this topology works for low power applications, due to the limitation on the value of primary inductance of the flyback transformer. Z-source inverter has been proposed in [11]. The topology gives ac output voltage which is greater or lower in magnitude compared to the input dc voltage. It uses the short-through state of the inverter bridge in order get the required gain. However, its main drawback is the impedance network, which increases size and cost of the converter. Wang et al., proposed a buck-boost principle based topology in [12]. In this topology, more number of devices conduct at a given instant, which results in more conduction losses.

Sachin et al., proposed a two inductor topology based on buck-boost principle in [13]. This topology has several advantages like less number of switches (four), low switching losses (only two switches out of four operate at high frequency) and compact size. The drawback of the topology is that it has limited

gain. A SSCS proposed in [14] can work in buck, boost or buck-boost mode to give ac output voltage. Even though this topology has advantages like modularity, compactness and low cost, it suffers from limited gain. A doubly grounded topology based on buck-boost principle is proposed in [15], which is compact and uses less number of components, however it gives low gain. A four switch topology based on buck-boost principle is proposed in [16]. This topology uses more number of components and gives less gain. Another coupled inductor based converter scheme was presented in [17] gives relatively more gain, but due to the leakage inductance problems, it is limited to low power applications only.

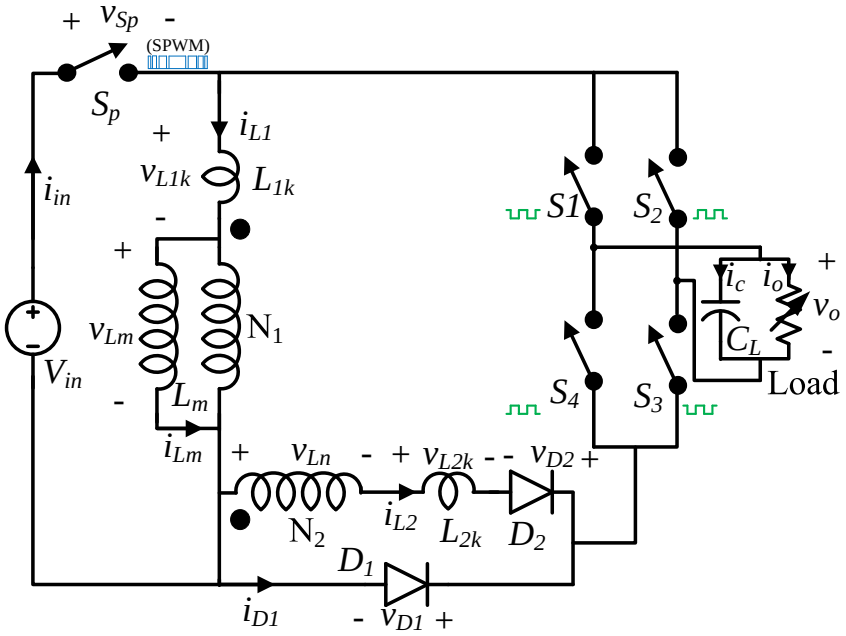


Figure 1: Proposed converter topology.

A single stage high gain topology using coupled inductor is proposed in [18]. This converter scheme has several advantages like less number of components and high gain. Due to the leakage inductance associated with coupled inductor, the topology is suitable only for low power applications. Normally when coupled inductors are used in power converters, the leakage inductance with them causes several undesirable effects like high voltage stress and energy loss. Several converter topologies, which can mitigate the adverse effects of leakage inductance are proposed in [19–23]. The converter presented in [23] has several desirable features like less number of components, high gain and does not require any additional capacitors to trap leakage energy. Therefore, this topology is used as a part of single stage conversion scheme presented in this paper. A single stage high gain buck-boost inverter using a

single coupled inductor is presented in this paper, which is shown in Fig. 1. The proposed converter has following advantages:

1. The topology gives high gain due to the use of coupled inductor, which makes this topology works better even in low input voltage conditions.
2. Only one active switch out of five operates at high frequency, thus its operation gives less switching loss.
3. No bulky capacitors are required to capture leakage energy associated with the coupled inductor, which in turn results in compact size.
4. The topology operation requires simple sinusoidal pulse width modulation (SPWM), hence avoids complex modulation techniques.
5. As coupled inductor is used instead of two inductors, core requirements and space requirements will be reduced.

Circuit Configuration		Components				Number of active switches operating at high frequency in an half cycle of output voltage	Number of switches contributing to conduction loss				Observations
		AS	PS	L	C		During inductor charging		During inductor discharging		
							AS	PS	AS	PS	
Un coupled inductor topologies	Caceres [8]	4	0	2	2	4	2	0	2	0	More conduction loss,more switching loss and EMI problems.
	Peng [11]	4	0	2	2	2	2	0	2	0	Big in size due to passive components and complex in control.
	Wang [12]	4	2	2	1	1	2	0	1	1	Low EMI problems but more conduction loss.
	Sachin [13]	4	2	2	1	1	1	0	1	1	Low switching and low conduction loss but gives low gain.
	Patel [15]	5	3	1	1	2	2	0	2	2	Has drawbacks like limited gain and conduction loss.
	Shafeeq [16]	4	4	1	1	1	2	0	2	2	More number of switches and more conduction loss.
Coupled inductor topologies	Yris [17]	4	2	2	1	1	1	0	1	1	High gain but suffers from harmful effects due to leakage inductance.
	High gain buck boost inverter[18]	4	2	1	1	1	1	0	1	1	High gain and compact converter but suffers from harmful effects due to leakage inductance.
	Proposed topology	5	2	1	1	1	1	0	2	1	High gain, low switching loss and free from leakage inductance harmful effects.

AS- Active switches, PS- Passive switches, L- Inductors, C- Capacitors

Figure 2: A brief comparison of the proposed topology with the existing topologies.

A brief comparison of the proposed topology with the existing topologies is presented in Fig. 2. Circuit configuration and working of the proposed topology in each switching cycle time and in output voltage's

each period time is presented along with analytical waveforms in Section 2, which gives the complete idea about the converter operation. Mathematical analysis of the proposed topology is given in Section 3. Section 4 gives the design of proposed circuit topology parameters. Simulation results in Section 5 and experimental results in Section 6 are presented to validate the proposed idea, followed by the conclusion in Section 7.

2 Circuit Configuration and Working

The proposed topology as shown in Fig.1 consists of five active power switches (S_p, S_1, S_2, S_3 and S_4), two passive power switches, an output capacitor and a coupled inductor. Out of five switches, only switch (S_p) operates at high frequency and remaining four switches operate at frequency of output voltage. Diode (D_1) is mainly intended for shorting inductor (L_1) to the output voltage (v_o) when the switch (S_p) gets turned off, in turn it avoids the adverse effects of leakage inductance associated with the coupled inductor. The operation of the proposed topology is same and symmetrical in each switching cycle of both the half cycles of output voltage. Therefore, only a switching cycle of positive half cycle of output voltage is considered for explanation. **During positive half cycle of output voltage, switches (S_2 and S_4) are turned on and switches (S_1 and S_3) are turned off. Similarly, During negative half cycle of output voltage, switches (S_1 and S_3) are turned on and switches (S_2 and S_4) are turned off**. During each half cycle of output voltage, switch (S_p) operates with SPWM, ensuring transfer of power from input dc source to output ac load in each switching cycle.

Several assumptions are made in order to explain the steady state operation of the proposed topology. These assumptions are:

1. All parasitic components except leakage inductance of coupled inductor are neglected.
2. The on-state resistance of the switches and forward voltage drop of the diodes are ignored.
3. Capacitor (C_L) is large enough to be consider it as a constant voltage source over a switching cycle.
4. The topology is operating under continuous conduction mode (primary inductor current (i_{L1}) is operating in continuous conduction mode).

2.1 Mode 1 (t_0 to t_1)

By turning on switch (S_P), inductor (L_m) gets charged by source voltage (V_{in}) through switch (S_P). Diodes (D_1 and D_2) are reverse biased during this mode. Current in the mutual inductance (L_m) rises linearly with the slope of V_{in}/L_m. During this mode output capacitor (C_L) discharges through load. This mode of operation is shown in Fig. 3a.

2.2 Mode 2 (t_1 to t_2)

This mode starts when switch (S_p) is turned off. Both Diodes (D_1 and $D2$) become forward biased. The leakage energy associated with the leakage inductance (L_{1k}) will be delivered to the load through the diode (D_1) in this mode. The switch voltage (v_{Sp}) rises to $V_{in}+v_o$ as it is clamped between V_{in} and v_o. A voltage of ($-v_o - v_{L_m}$) will appear across leakage inductance (L_{1k}), which resets the leakage inductance (L_{1k}). Therefore, the current through leakage inductance (L_{1k}) decreases with a slope of ($\frac{-v_o - v_{L_m}}{L_{1k}}$). In the same time, current (i_{L2}) starts to increase. The difference of these currents will be taken by the diode (D_1) during this interval. At the end of this interval, diode (D_1) becomes reverse biased. This mode ends when currents in both inductors become equal. Fig. 3b gives this mode of operation.

2.3 Mode 3 (t_2 to t_3)

In this mode, diode (D_1) becomes reverse biased and both inductors (L_1 and L_2) come in series and supply power to the load. The current in both leakage inductors is same and starts decreasing. This mode ends when the switch (S_p) is turned on again. In this mode, the output voltage appears across each inductor as per number of turns. This mode of operation is shown in Fig. 3c.

2.4 Mode 4 (t_3 to t_0)

When switch (S_p) is turned on, diode (D_1) is still in reverse biased condition. Diode (D_2) still continues to conduct due to the non-zero current in the leakage inductor (L_{2k}). Negative voltage across leakage inductor (L_{2k}) resets the current through it. This mode ends when the current in inductor L_{2k} becomes zero and diode (D_2) becomes reverse biased. The topology starts working again from mode 1. Fig. 3d gives this mode operation. Analytical waveforms of input current (i_{in}), current through each inductor

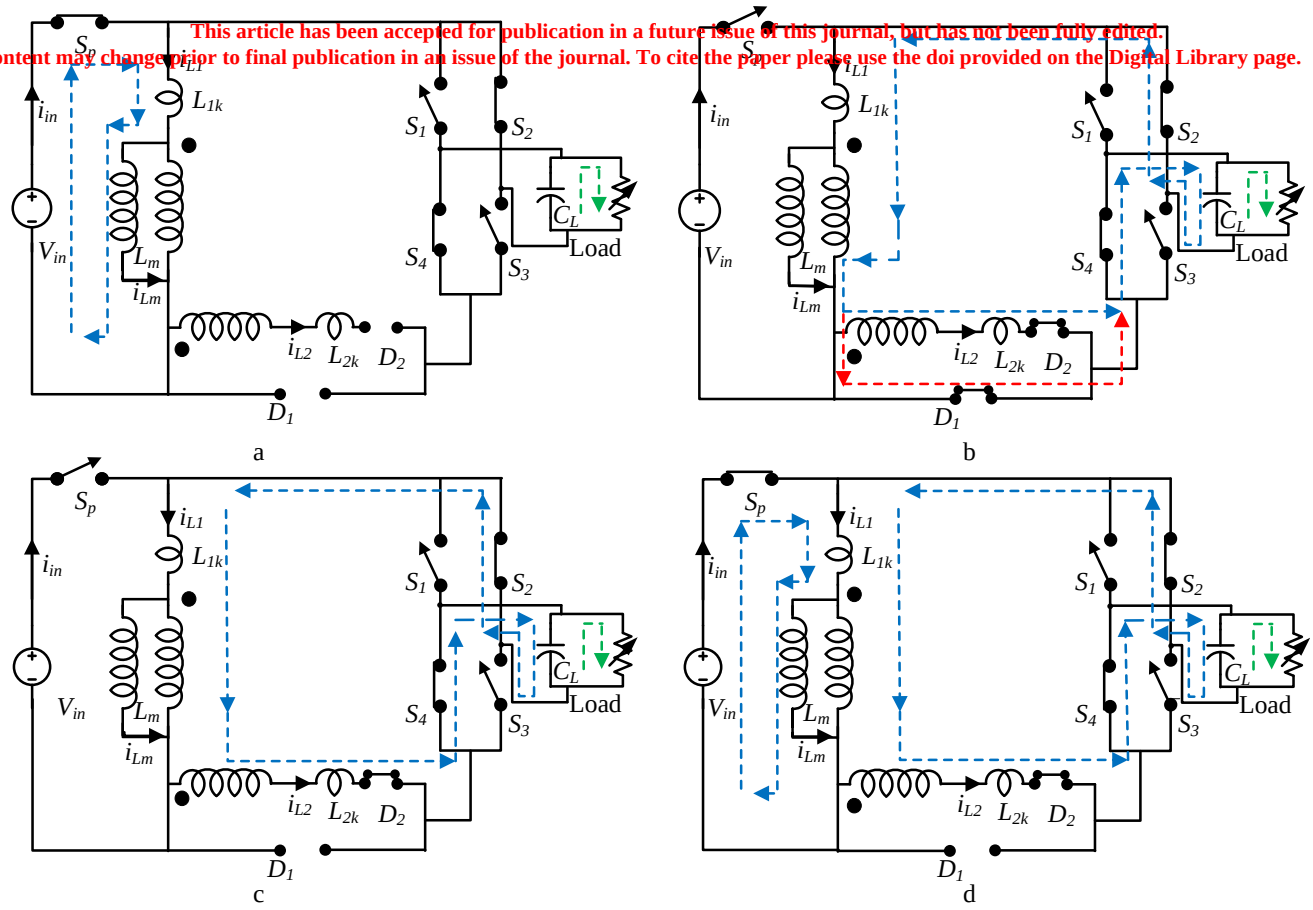


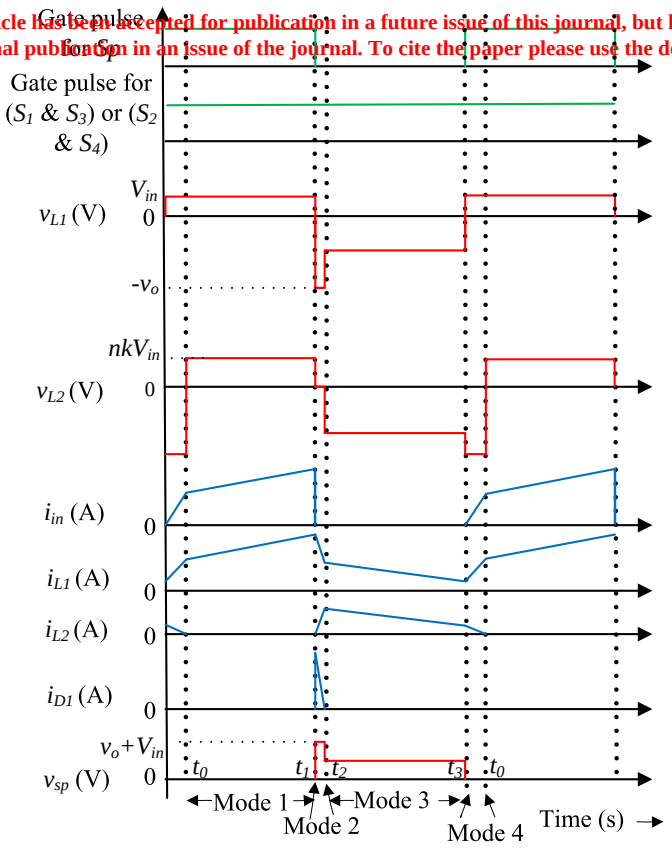
Figure 3: Modes of operation. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

(i_{L1} and i_{L2}), voltage across each inductor (v_{L1} and v_{L2}), current through diode D_1 (i_{D1}) and gating pulses over a switching cycle are as shown in Fig. 4a. In the same scheme, when the switch (S_p) is operated with SPWM with twice the output voltage frequency, resulting analytical waveforms as shown in Fig. 4b.

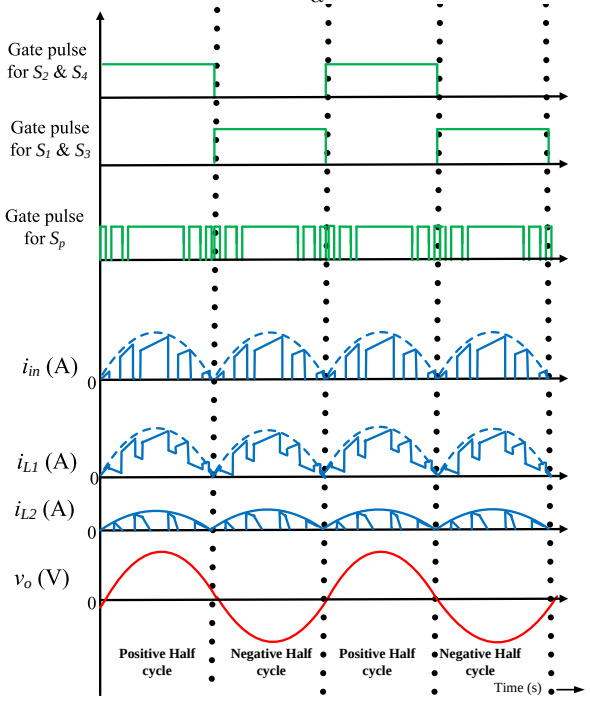
3 Mathematical Analysis

As proposed converter's operation is symmetrical and same in both half cycles of output voltage, so only one switching cycle of positive half cycle of output voltage is considered for analysis. In order to reduce the complexity associated with the circuit equations, following assumptions are made.

1. All parasitic components, on-state resistance of the active switches and forward voltage drop of the diodes are ignored.



a



b

Figure 4: Analytical waveforms of the proposed topology. (a) Analytical waveforms of the proposed topology over a switching cycle. (b) Analytical waveforms of the proposed topology over two full cycles output voltage.

2. Leakage inductance of the coupled inductor is only considered in voltage gain calculation and in remaining parts, it is neglected in order to simplify calculations.

3. Capacitor (C_L) is large enough to be considered as constant voltage source over a switching cycle.

4. Since, Mode 2 interval time is very less compared to switching period, that can be discarded for calculating the voltage gain.

3.1 Voltage Gain

Let N_1, N_2 be the number of turns on primary and secondary and $n = (N_2/N_1)$ for the topology shown in Fig.1. Let L_1 be the primary inductance, therefore inductance L_2 can be written as following [24].

$$L_2 = n^2 L_1.$$

L_1 can be written as

$$L_1 = L_m + L_{1k}.$$

Where L_{1k} is leakage inductance associated with primary winding, L_m is magnetizing inductance. Coefficient of coupling (k) is defined as following.

$$k = \left(\frac{L_m}{L_m + L_{1k}}\right).$$

During switch on time, voltage across magnetizing inductance (v_{Lm}) is given as

$$v_{L_m} = kV_{in}.$$

During switch off time, relation between current through magnetizing inductance (i_{Lm}) and current through leakage inductance (i_{L1}) is given as following.

$$i_{L_m} = (1+n)i_{L_1}. \tag{1}$$

Further, the relation between output voltage (v_o) and voltages across inductors (v_{L1} and v_{L2}) can be written as

$$v_{L_1} + v_{L_2} = -v_o. \tag{2}$$

Where

$$v_{L_1} = v_{L_m} + v_{L_{1k}} \text{ and } v_{L_2} = v_{Ln} + v_{L2k} = nv_{L_m} + n^2 v_{L_{1k}}.$$

Substituting v_{L_1}, v_{L_2} in (2).

$$(1+n)v_{L_m} + (1+n^2)v_{L_{1k}} = -v_o. \tag{3}$$

From (1), v_{L_m} can be written as

$$v_{L_m} = L_m \frac{di_{L_m}}{dt} = (1+n)L_m \frac{di_{L_1}}{dt}. \tag{4}$$

Thus, from (4), $v_{L_{1k}}$ can be written as

$$v_{L_{1k}} = L_{1k} \frac{di_{L_1}}{dt} = \frac{L_{1k}}{(1+n)L_m} v_{L_m} = \frac{1-k}{(1+n)k} v_{L_m}. \tag{5}$$

Substituting (5) into (3) will give the following equation.

$$v_{L_m} = \frac{(1+n)k}{(n^2+2nk+1)}(-v_o). \tag{6}$$

Applying Volt-Sec balance across mutual inductance (L_m) gives

$$v_{L_m} = kV_{in}d + \frac{-v_o(1+n)k}{(n^2+2nk+1)}(1-d) = 0.$$

Where d is duty cycle. Solving the above equation gives

$$\frac{v_o}{V_{in}} = \left(\frac{d}{1-d}\right)\frac{(n^2+2nk+1)}{(1+n)} = M(d). \tag{7}$$

Using above equation, study state gain curves are plotted with $k = 0.95$ for different values of n. These curves are shown in Fig. 5. Comparison of steady state gain curves of the proposed scheme with the scheme presented in [13] is made in the Fig. 5. When $k = 1$, equation (7) becomes

$$\frac{v_o}{V_{in}} = \frac{d}{1-d}(1+n) = M(d). \tag{8}$$

From above equation, In order to get output voltage (V_o) of frequency ω rad/s from input voltage (V_{in}), duty cycle can be varied as per the following equation.

$$d(t) = \left(\frac{v_o sin(wt)}{(1+n)V_{in} + v_o sin(wt)}\right). \tag{9}$$

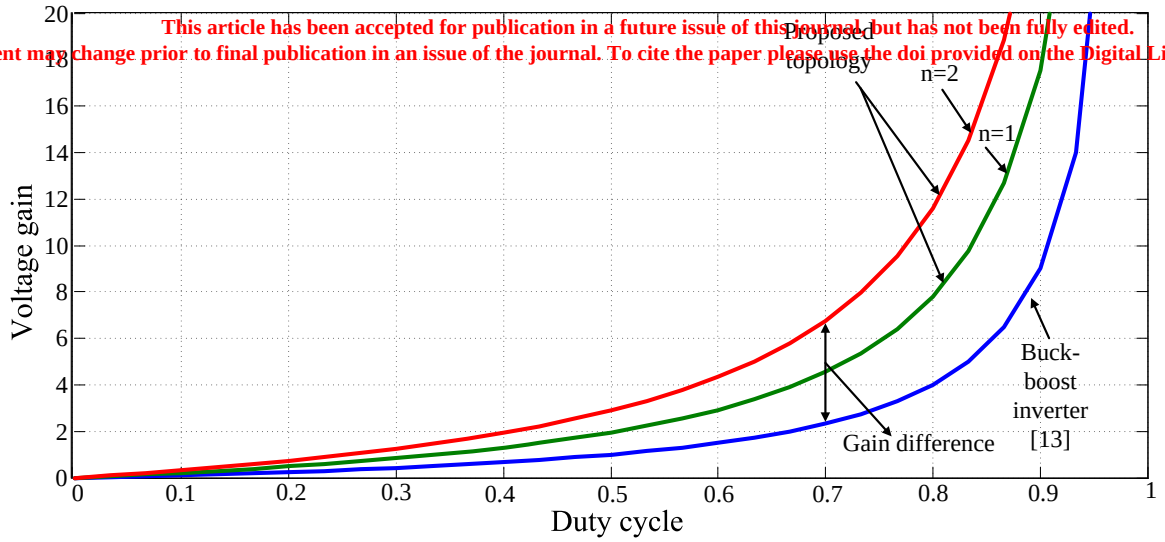


Figure 5: Steady state gain curves

3.2 Voltage Stress Across the Switches

3.2.1 For Switch S_p

The maximum voltage stress across the active switch (S_p) occurs during Mode 2, i.e. when the switch (S_p) turns off. The switch (S_p) clamps between input and output terminals. Hence the maximum voltage stress across the active switch (S_p) is

$$v_{S_{p(max)}} = V_{in} + v_{o(max)} \tag{10}$$

3.2.2 For Switches S_1, S_2, S_3 and S_4

The maximum voltage stresses across the active switches (S_1, S_2, S_3 and S_4) are same and occur at peak value of output voltage. Therefore, the maximum stress across these switches is $v_{o(max)}$.

3.2.3 For Diode D_1

The maximum voltage across it occurs during Mode 1 and Mode 4. In these modes, the diode clamps between $V_{in} + v_o$. Therefore, the maximum voltage across diode (D_1) is

$$v_{D_{1(max)}} = V_{in} + v_{o(max)} \tag{11}$$

3.2.4 For Diode D_2

For diode D_2, the maximum voltage across it occurs in Mode 1. Maximum voltage across it is given by

$$v_{D_2} = v_{L_1} + v_{L_2} + v_o \tag{12}$$

$$v_{D_{2(max)}} = [(1+n) * V_{in}] + v_{o(max)} \ . \tag{13}$$

4 Design of the Components

The design of proposed topology for CCM operation requires determination of the values of coupled inductor and output capacitor (C_L).

4.1 Design of Coupled Inductor

Let ΔI_{L1} be the allowable current rise from nominal current through inductor (L_1). From Fig. 6, voltage across inductor (L_1) during Δt_{on} can be written as [25]

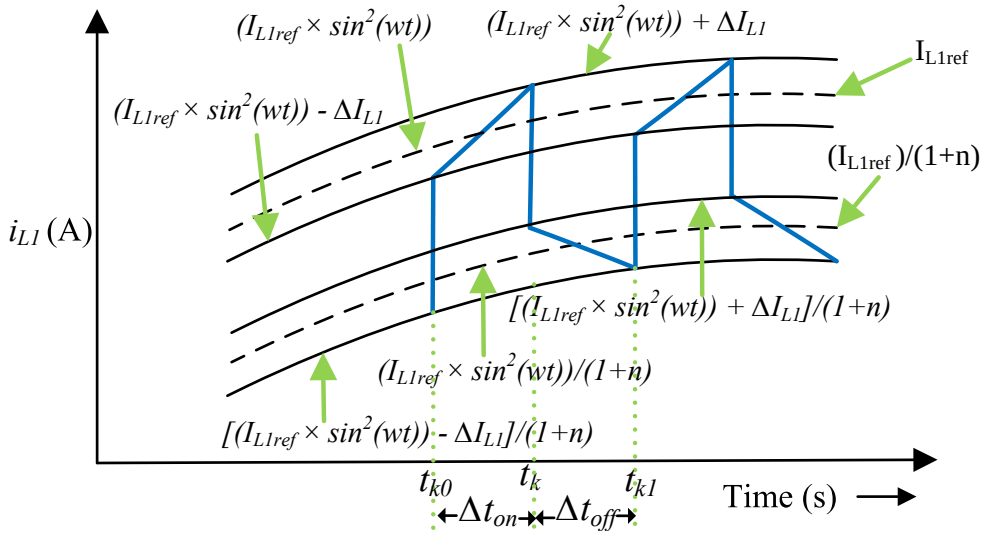


Figure 6: A section of primary inductor (L_1) current waveform.

$$\frac{V_{in}}{L_1} = \left(\frac{(I_{L1ref} \times sin^2(wt_{k0})) + \Delta I_{L1}}{t_k - t_{k0}}\right) - \left(\frac{(I_{L1ref} \times sin^2(wt_k)) - \Delta I_{L1}}{t_k - t_{k0}}\right) \tag{14}$$

$$\frac{V_{in}}{L_1} = \frac{(I_{L1ref} \times (sin^2(wt_{k0}) - sin^2(wt_k))) + (2 \times \Delta I_{L1})}{t_k - t_{k0}}. \tag{15}$$

Where, V_{in} is the average input voltage which appears across the inductor (L_1) during switch on time. Time intervals t_{k0}, t_k are switching instants as shown in the figure. Assuming $t_k - t_{k0} = \Delta t_{on}$, $sin(\omega(t_k - t_{k0})) \approx (\omega \times \Delta t_{on})$, $t_{k0} + t_k = 2t_k$ and simplifying equation (15), gives the following.

$$\frac{V_{in}}{L_1} = \frac{(-I_{L1ref} \times sin(2wt_k) \times \omega \times \Delta t_{on}) + (2 \times \Delta I_{L1})}{\Delta t_{on}} \tag{16}$$

$$\Delta t_{on} = \frac{2 \times \Delta I_{L1} \times L_1}{V_{in} + I_{L1ref} \times sin(2\omega t_k) \times \omega \times L_1}. \tag{17}$$

Similarly, Δt_{off} time can be calculated as

$$\Delta t_{off} = \frac{2 \times \Delta I_{L1} \times (1+n) \times L_1}{V_o + I_{L1ref} \times sin(2\omega t_k) \times \omega \times (1+n) \times L_1}. \tag{18}$$

Total switching period (T_s) is given by

$$\begin{aligned} T_s = \Delta t_{on} + \Delta t_{off} =& 2 \times \Delta I_{L1} \times L_1 \times \left(\frac{1}{v_o + I_{L1ref} \times sin(2\omega t_k) \times \omega \times L_1} \right) \\ &+ 2 \times \Delta I_{L1} \times L_1 \times \left(\frac{1}{v_o + I_{L1ref} \times sin(2\omega t_k) \times \omega \times (1+n) \times L_1} \right). \end{aligned} \tag{19}$$

At the peak of the output voltage where $sin(2\omega t_k) \approx 0$ and $sin(\omega t_k) \approx 1$, equation (19) can be simplified as following.

$$T_s = L_1 \times \left(\frac{2 \times \Delta I_{L1}}{V_{in}} \right) + L_1 \times \left(\frac{2 \times \Delta I_{L1} \times (1+n)}{v_{o(max)}} \right). \tag{20}$$

From above equation, L_1 can be written as

$$L_1 = \frac{T_s \times V_{in} \times v_{o(max)}}{2 \times \Delta I_{L1} \times [V_{in}(1+n) + v_{o(max)}]}. \tag{21}$$

After calculating L_1, L_2 can be expressed as following.

$$L_2 = n^2 \times L_1. \tag{22}$$

4.2 Design of Capacitor (C_L)

The value of the maximum energy that can be transferred through coupled inductor decides the value of output capacitance (C_L). Assuming unity power factor operation, maximum energy transferred from input to output at the peak of the output voltage. By equating the decrease in energy of the coupled inductor with the increase in the energy of output capacitor, the result is as follows.

$$\begin{aligned} &\frac{1}{2} \times L_1 \frac{(1+n^2+2n)}{1+n} [(I_{L1ref(max)} + \Delta I_{L1})^2 - (I_{L1ref(max)} - \Delta I_{L1})^2] \\ &= \frac{1}{2} \times C_L [(v_{o(max)} + \Delta v)^2 - (v_{o(max)} - \Delta v)^2]. \end{aligned} \tag{23}$$

Simplification of above equation gives the capacitance value as following.

$$C_L = \frac{L_1 \times (1+n) \times I_{L1ref(max)} \times \Delta I_{L1}}{v_{o(max)} \times \Delta v}. \quad (24)$$

Where, $I_{L1ref(max)}$ is the maximum amplitude of the reference primary inductor current corresponding to rated output power and Δv is the maximum allowable ripple voltage across output capacitor (C_L).

4.3 Control Technique

In this paper, double-loop control presented in [26] is used for controlling both output voltage and current in inductor (L_1). Control block diagram of proposed converter is shown in Fig. 7. As per double loop control, voltage control loop (outer loop) for the proposed converter is derived and is shown in Fig. 8. Similarly, current control loop (inner loop) for the proposed converter is derived and is shown in Fig. 9. Here r_{L1} and r_c are the equivalent series resistances associated with L_1 and C_L. In both simulation and experimental conditions, inner loop controllers are tuned for 4 kHz bandwidth with 60^0 phase margin and outer loop controllers are tuned for 2 kHz bandwidth with 60^0 phase margin.

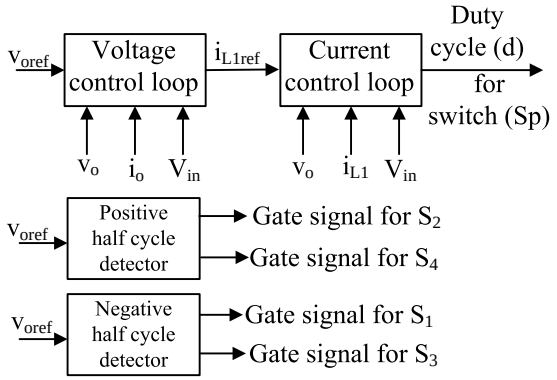


Figure 7: Control block diagram of proposed converter

5 Simulation Studies

The Proposed 2 kW converter topology is simulated using MATLAB/SIMULINK and the parameters used are shown in Table 1. First, this proposed topology is tested with the resistive load mentioned in Table 1, and corresponding results are shown in Fig. 10. Gating pulses for all the active switches are shown in Fig. 10a. From the switching pulses in Fig. 10a, it is evident that only one switch (S_p) will be

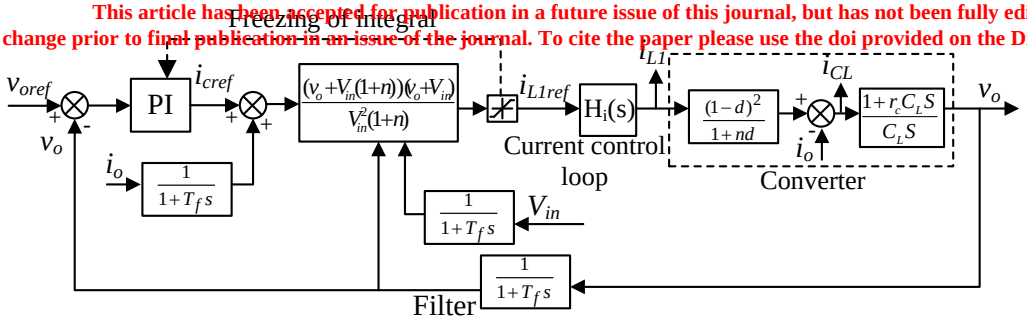


Figure 8: Voltage control loop (outer loop)

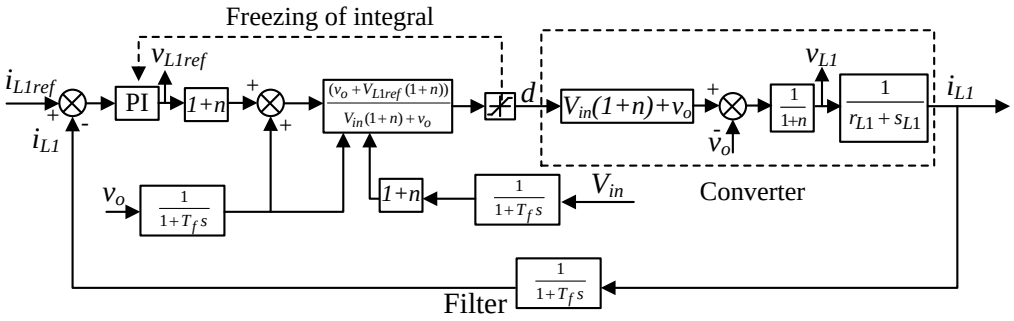


Figure 9: Current control loop (inner loop)

Table 1: Simulation Parameters

Parameters	**Value**
Input voltage (V_{in})	48 V
Output voltage (V_o)	230 V (RMS)
Output voltage frequency	50 Hz
Switching frequency (for S_p)	50 kHz
Inductor (L_1)	30 μH
Inductor (L_2)	120 μH
Coefficient of coupling (k)	0.95
Output capacitor (C_L)	30 μF
Resistive load	26.45 Ω
R-L load	30 Ω, 2 mH

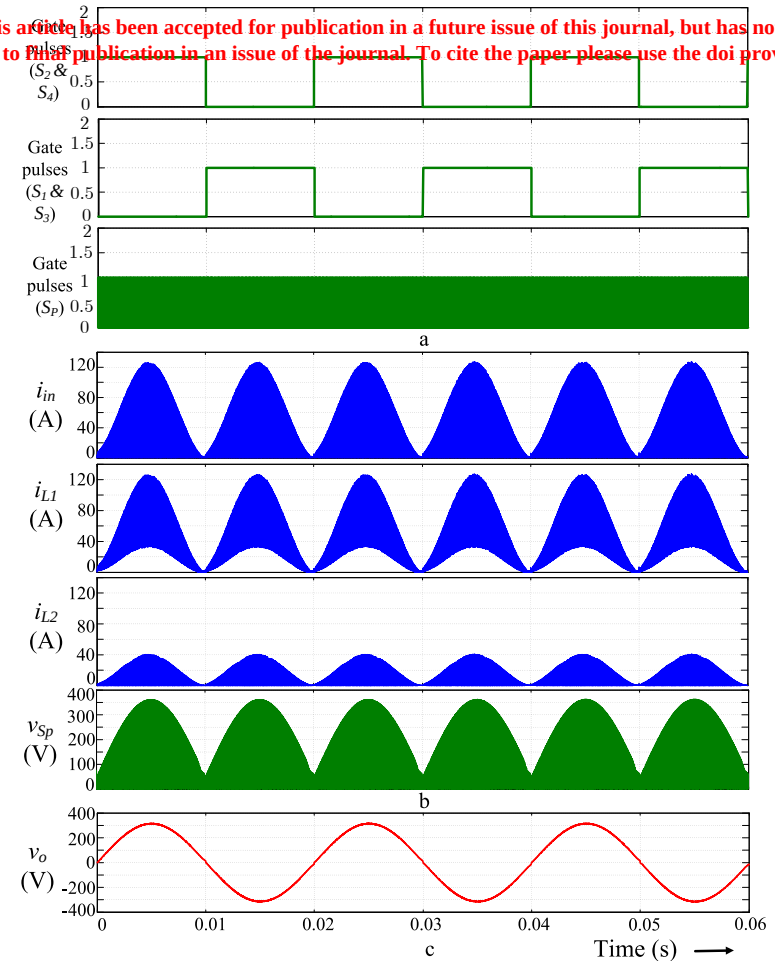


Figure 10: Steady state simulation results of proposed topology for resistive load. (a) Pulses for active switches ($S_p, S_1 - S_4$). (b) Currents (i_{in}, i_{L1}, i_{L2}) and voltage across switch S_p (v_{Sp}). (c) Output voltage (v_o).

operated at higher frequency out of all switches. Input source current (i_{in}), current through inductors (i_{L1} and i_{L2}), and voltage across switch (v_{Sp}) are shown in Fig. 10b. As seen from Fig. 10b, all currents are varying in rectified sinusoidal manner in each full cycle of output voltage. Input current (i_{in}) and secondary inductor current (i_{L2}) are always discontinuous. Primary inductor current (i_{L1}) is combination of 50 Hz rectified sine wave and high frequency (50 kHz) ripple, which can be evident from the Fig. 10b. The waveform of voltage across switch (v_{Sp}) clearly indicates the alleviation of harmful effects of the leakage inductance associated with coupled inductor. The output voltage (v_o) of the proposed converter topology is shown in Fig. 10c. Now, the proposed converter topology is tested with an R-L load listed in Table 1. Simulation results corresponding to R-L load are shown in Fig. 11. Switching pulses for all

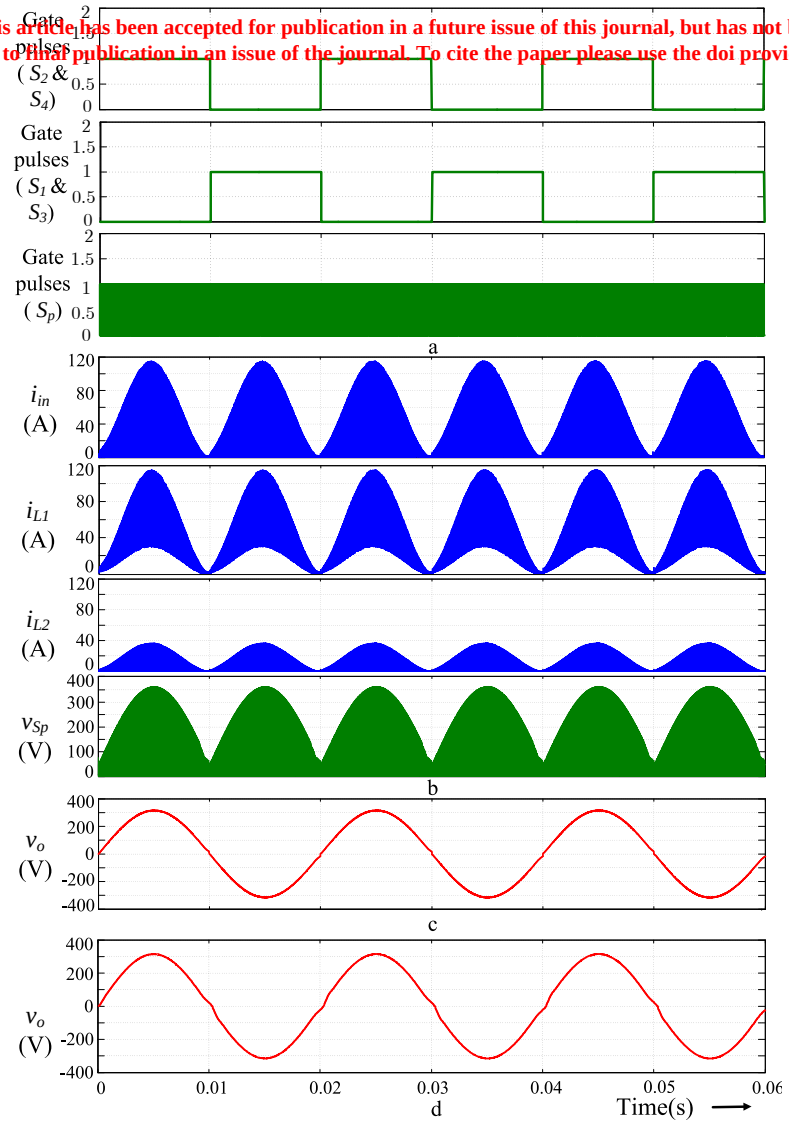


Figure 11: Steady state simulation results of proposed topology (a) Pulses for active switches (S_p, S_1-S_4). (b) Currents (i_{in}, i_{L1}, i_{L2}) and voltage across switch S_p (v_{Sp}) for R-L load. (c) Output voltage (v_o) waveform for R-L load. (d) Output voltage (v_o) waveform for non-linear load.

active switches are shown in Fig. 11a, input source current (i_{in}), current through inductors (i_{L1} and i_{L2}), and voltage across switch (v_{Sp}) are shown in Fig. 11b and output voltage (v_o) of the proposed converter is shown in Fig. 11c. Similarly, the topology is tested with non-linear (single phase rectifier with R-L load (mentioned in Table 1)) load and obtained output voltage waveform is shown in Fig. 11d.

6 Experimental results

Table 2: Experimental Setup Parameters

Parameters	**Value**
Input voltage (V_{in})	60 V
Output voltage (V_o)	230 V (RMS)
Output voltage frequency	50 Hz
Switching frequency (for S_p)	50 kHz
Inductor (L_1)	0.45 mH
Inductor (L_2)	1.9 mH
Coefficient of coupling (k)	0.95
Output capacitor (C_L)	2 μF
Resistive load	529 Ω
R-L load	600 Ω, 2 mH

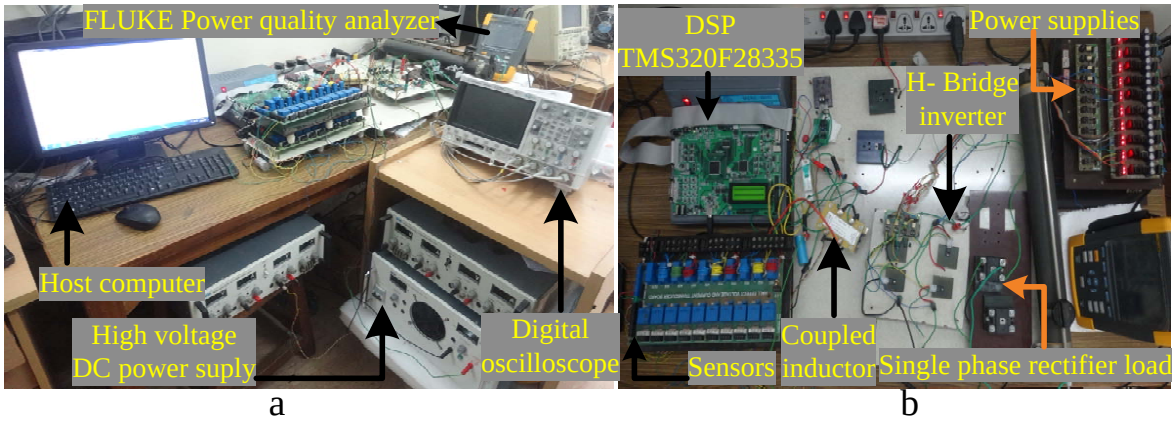


Figure 12: (a) Experimental setup, (b) Zoomed view

To validate the proposed scheme, a 100 W prototype was developed in the laboratory. A power MOSFET (K16E60W) is used for implementing switch (S_p). Diodes ($D1$ and D_2) are implemented using power diodes (MSR1560). Power IGBTs (STGF7NB60SL) are used for implementing switches (S_1, S_2, S_3 and S_4). TMS320F28335 DSP controller is used to give corresponding switching pulses to all active switches. Circuit parameters are designed as per aforementioned design rules. Circuit parameters

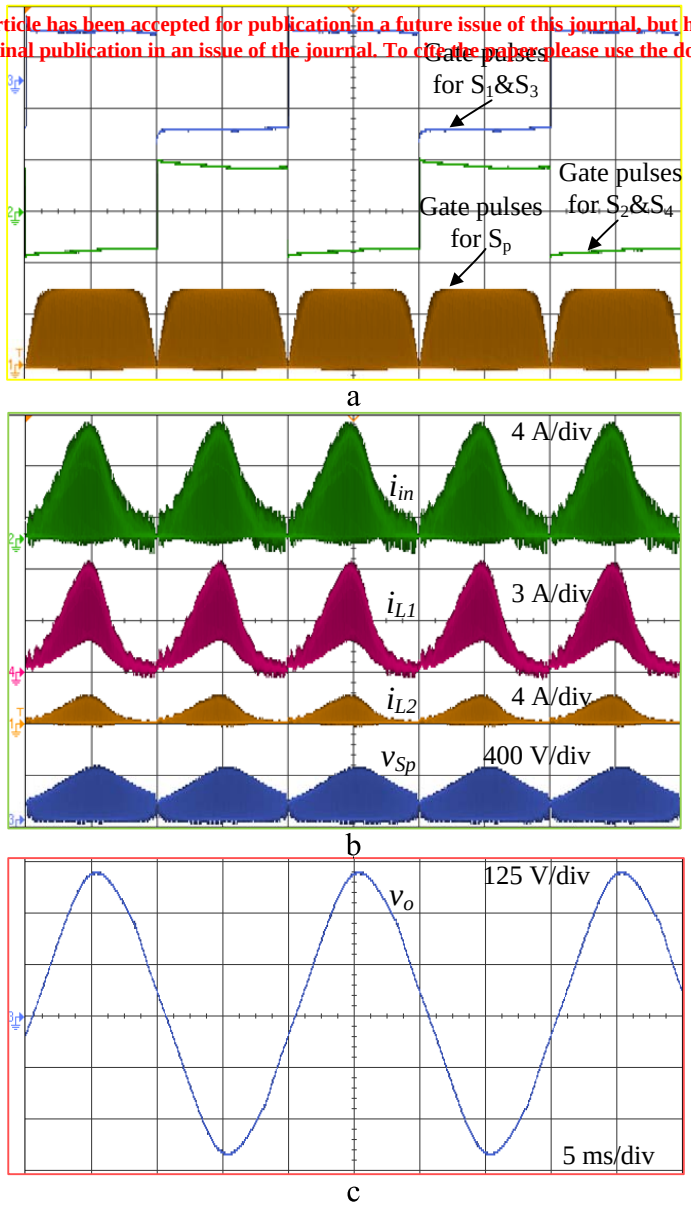


Figure 13: Steady state experimental results of proposed topology for resistive load. (a) Pulses for active switches ($S_p, S_1 - S_4$). (b) Currents (i_{in}, i_{L1}, i_{L2}) and voltage across switch S_p (v_{Sp}). (c) Output voltage (v_o).

used in experimental conditions are shown in Table 2. Developed experimental setup is shown in Fig. 12a, and its zoomed view is shown in Fig. 12b. The output capacitance (C_L) is taken as 2μF. Firstly, the hardware setup is tested with resistive load ($529\,\Omega$), the corresponding results are shown in Fig. 13. Switching pulses given for active switches are shown in Fig. 13a. Input current from source (i_{in}), inductor currents (i_{L1}, i_{L2}) and voltage across switch (v_{Sp}) are shown in Fig. 13b. Fig. 13c gives voltage

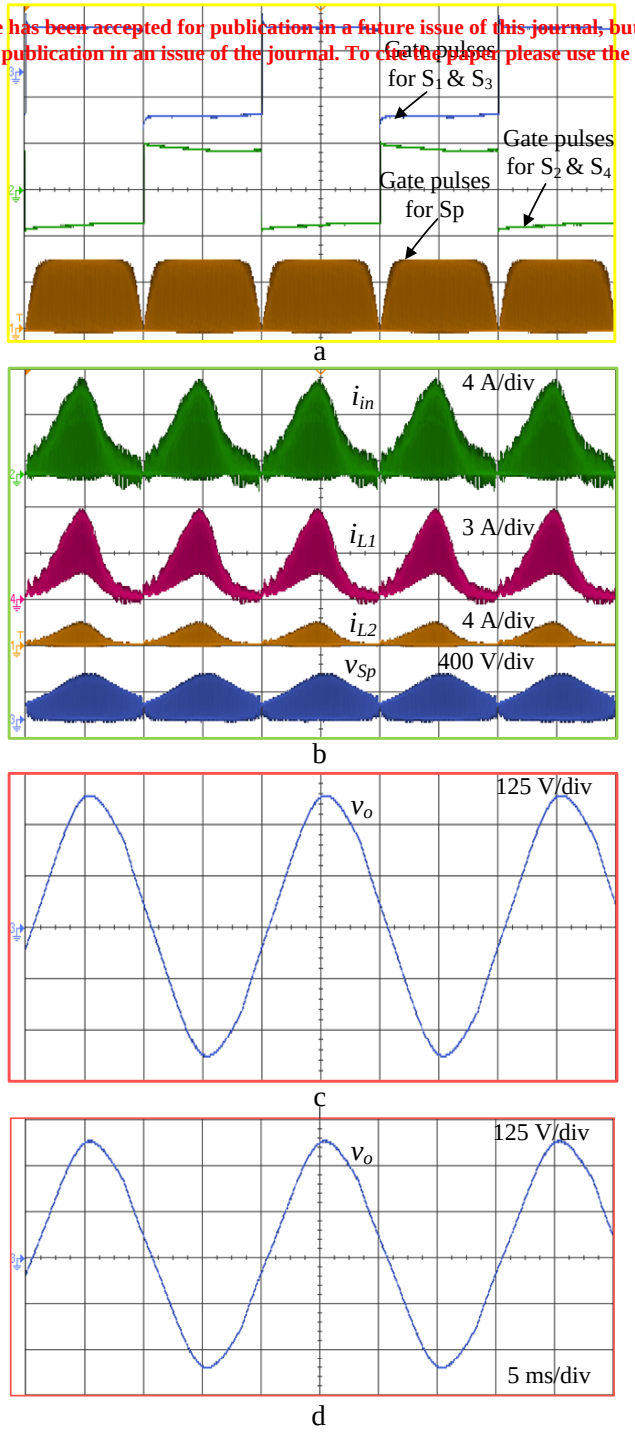


Figure 14: Steady state experimental results of proposed topology. (a) Pulses for active switches ($S_p, S_1 - S_4$). (b) Currents (i_{in}, i_{L1}, i_{L2}) and voltage across switch S_p (v_{Sp}) for R-L load. (c) Output voltage (v_o) for R-L load. (d) Output voltage (v_o) for non linear load.

obtained across the load after using low pass filter. The obtained efficiency of the proposed converter with resistive load is 86 %. This may be due to non optimization of circuit parameters. Secondly, the proposed topology is tested with R-L load (600 Ω and 2 mH) and the obtained results are shown in Fig. 14. Switching pulses given for active switches are shown in Fig. 14a, currents in the proposed topology (i_{in}, i_{L1}, i_{L2}) are shown in Fig. 14b and output voltage across the load after using low pass filter is shown in Fig. 14c. Similarly, the topology is tested with non-linear load (single phase rectifier with R-L load (mentioned in Table 2)) and obtained output voltage waveform is shown in Fig. 14d. The obtained experimental results are in close agreement with both simulation and analytical results, hence validate the proposed scheme. Whenever required output voltage is greater than input voltage, it acts as boost converter and when required output voltage is lesser than input voltage, it acts like buck converter. Both buck and boost operations are implemented in each half cycle of output voltage. This can be verified by output voltage experimental waveforms for each load. THD measurement is done using

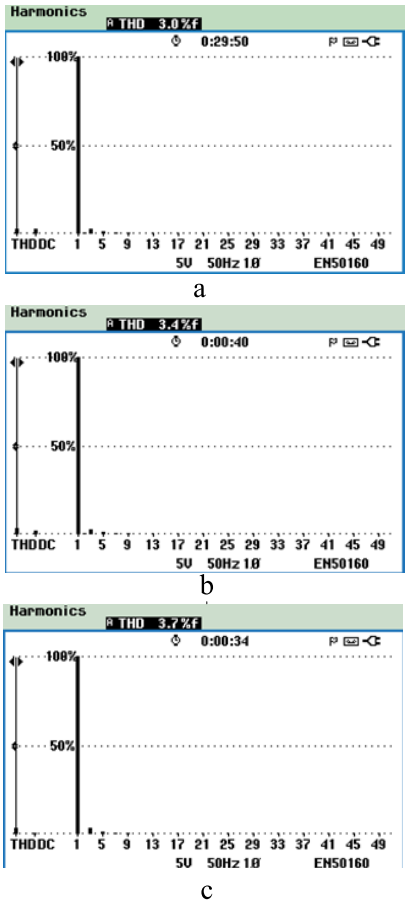


Figure 15: Harmonic spectrum of output voltage for (a) R load. (b) R-L load. (c) Non-linear load.

FLUKE Power Quality Analyzer. THDs of the obtained output voltage waveform for resistive load, R-L load and non-linear load are 3.0%, 3.4% and 3.7% respectively. Harmonic spectrum of output voltage for the tested loads are shown in Fig. 15.

7 Conclusion

In this paper a high gain single stage buck-boost dc-ac inverter topology is proposed. This topology has advantages such as high gain, low switching loss and compact in size. Operation principle of the proposed topology is explained with analytic details and complete design of the topology components is presented. From the mathematical analysis, it is observed that the topology provides high gain and performs dc-ac power conversion in single stage. This observation has confirmed by detailed simulation and experimental studies. The detailed simulation and experimental results demonstrate the effectiveness of topology in terms of high gain and free from harmful effects of leakage inductance. Due to these features the proposed topology with input side passive filter can be used effectively in transferring the power from applications like photovoltaics, where source output voltage(dc) varies with time.

ACKNOWLEDGEMENTS

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APPENDIX

Table 3: Experimental Coupled Inductor Parameters

Parameters	**Value**
Core type	E65/32/27
Area product of the core	213000 mm^4
Type of conductor used for both inductors	Enameled copper (SWG22)
Number of turns wounded for inductor (L_1)	24
Number of turns wounded for inductor (L_2)	48

References

[1] D. Binu Ben Jose, N. Ammasai Gounden, and J. Ravishankar: 'Simple power electronic controller for photovoltaic fed grid-tied systems using line commutated inverter with fixed firing angle,' *IET Power Electron.*, 2014, 7, (6), pp. 1424–1434.

[2] M. Villalva, T. de Siqueira, and E. Ruppert: 'Voltage regulation of photovoltaic arrays: small-signal analysis and control design,' *IET Power Electron.*, 2010, 3, (6), pp. 869–880.

[3] Jinn-Chang Wu, Kuen-Der Wu, Hurng-Liahng Jou and Sheng-Kai Chang: 'Small-capacity grid-connected solar power generation system,' *IET Power Electron.*, 2014, 7, (11), pp. 2717-2725.

[4] Yu, X. and Starke, M.R. and Tolbert, L.M. and Ozpineci, B.: 'Fuel cell power conditioning for electric power applications: a summary,' *IET Electric Power Applications*, 2007, 1, (5), pp. 643-656.

[5] Meneses, D. and Blaabjerg, F. and Garcia, O. and Cobos, J.A: 'Review and comparison of step-up transformerless topologies for photovoltaic AC-module application,' *IEEE Power Electron.*, 2013, 28, (6), pp. 2649-2663.

[6] M. Hanif, M. Basu, and K. Gaughan: 'Understanding the operation of a z-source inverter for photovoltaic application with a design example,' *IET Power Electron.*, 2011, 4, (3), pp. 278–287.

[7] M.-K. Nguyen, T.-V. Le, S.-J. Park, Y.-C. Lim, and J.-Y. Yoo: 'Class of high boost inverters based on switched-inductor structure,' *IET Power Electron.*, 2015, 8, (5), pp. 750–759, 2015.

[8] Caceres, R.O. and Barbi, I,: 'A boost DC-AC converter: analysis, design, and experimentation,' *IEEE Power Electron.*, 1999, 14, (1), pp. 134-141.

[9] Kasa, N. and Lida, T. and Iwamoto H.: 'Maximum power point tracking with capacitor identifier for photovoltaic power system,' in *Proc. IEE Electric Power Applications conf.*, November 2000, pp. 497-502.

[10] Kasa, N. and Iida, T.: 'Flyback type inverter for small scale photovoltaic power system,' in *Proc. IEEE Industrial Electronics Society Annual Conf (IECON).*, November 2002, pp. 1089-1094.

[11] F. Z. Peng: 'Z-source inverter,' *IEEE Trans. Industry Applications*, 2003, 39, (2), pp. 504-510.

[12] C.-M. Wang: 'A novel single-stage full-bridge buck-boost inverter,' *IEEE Trans. Power Electron.*, 2004, 19, (1), pp. 150–159.

[13] S. Jain and V. Agarwal: 'A single-stage grid connected inverter topology for solar pv systems with maximum power point tracking,' *IEEE Trans. Power Electron.*, 2007, 22, (5), pp. 1928–1940.

[14] B. Prasad, S. Jain, and V. Agarwal: 'Universal single-stage grid-connected inverter,' *IEEE Trans. Energy Conversion*, 2008, 23, (1), pp. 128–137.

[15] H. Patel and V. Agarwal: 'A single-stage single-phase transformer-less doubly grounded grid-connected PV interface,' *IEEE Trans. Energy Conversion*, 2009, 24, (1), pp. 93–101.

[16] K. Shafeeque and P. Subadhra: 'A novel single-phase single-stage inverter for solar applications,' in *Proc. IEEE Advances in Computing and Communications (ICACC) conf.*, August 2013, pp. 343-346.

[17] J. Yris, H. Calleja, L. Hernandez, and J. Olmos: 'Design and analysis of a grid-connected inverter without isolation for an ac module,' in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC) conf.*, February 2012, pp. 2095-2099.

[18] T. Sreekanth, N. Narasamma, and M. Mishra: 'A single stage high gain buck-boost inverter with coupled inductor,' in *proc. IEEE Power Electronics, Drives and Energy Systems (PEDES) Conf.*, December 2014, pp. 1-5.

[19] K. Tseng and T. Liang: 'Novel high-efficiency step-up converter,' *IEE. Electric Power Applications*, 2004, 151, (2), pp. 182–190.

[20] R.-J. Wai and R.-Y. Duan: 'High step-up converter with coupled-inductor" *IEEE Trans. Power Electron.*, 2005, 20, (5), pp. 1025-1035.

[21] Y. Berkovich and B. Axelrod: 'Switched-coupled inductor cell for dc-dc converters with very large conversion ratio,' *IET. Power Electron.*, 2011, 4, (3), pp. 309-315.

[22] M.-H. Keum, Y. Choi, S.-K. Han, and J. il Kang: 'High efficiency voltage-clamped coupled-inductor boost converter,' in *Proc. IEEE Industrial Electronics Society (IECON) conf.*, November 2013, pp. 828-833.

[23] Y. Berkovich and B. Axelrod: 'High step-up dc-dc converter with coupled inductor and reduced switch-voltage stress" in *Proc. IEEE Industrial Electronics Society (IECON) conf.*, October 2012, pp. 453-458.

[24] L.-S. Yang, T.-J. Liang, H.-C. Lee, and J.-F. Chen: 'Novel high step-up dc-dc converter with coupled-inductor and voltage-doubler circuits,' *IEEE Trans. Industrial Electron.*, 2011, 58, (9), pp. 4196-4206.

[25] S. Jain and V. Agarwal: 'New current control based MPPT technique for single stage grid connected PV systems,' *Elsevier Energy Conversion and Management*, 2007, 48, (2), pp. 625 - 644, 2007.

[26] P. Sanchis, A. Ursaea, E. Gubia, and L. Marroyo: 'Boost dc-ac inverter: a new control strategy,' IEEE Trans. Power. Electron., 2005, 20, (2), pp 343–353.