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Single Phase Current Source Inverter with Multi Loop Control for Transformer-less Grid -PV Interface

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***Abstract* – In this work, a modified single phase Current Source Inverter (CSI) with improved multi loop control is proposed for transformer-less grid-PV interface application. A split capacitor arrangement with the middle point connected to the grid neutral and a common mode choke are used to modify the conventional CSI structure, to attenuate the ground leakage current. The proposed control method permits the use of reduced value of dc side inductor by maintaining the quality of the grid current, as if a high value of input inductor is used. Furthermore, virtual resistance damping is incorporated in the control loop to reduce the effect of LC resonance without compromising the efficiency, thus proving the feasibility of using CSI for the grid interface. Rigorous study, analysis and validation of the modified CSI structure with the proposed control technique is carried out with exhaustive simulations and experiments. The experimental results on a 250W laboratory prototype using the controller TMS320F28335 prove the effectiveness of the proposed CSI structure and its control.**

***Index Terms*—Current Source Inverter (CSI), grid connected, leakage current, PV, ripple reduction, transformer-less, virtual damping.**

I. INTRODUCTION

The possibility of utilizing a single phase Current Source Inverter (CSI), as an interface between the Distributed Generation (DG) source and the utility supply, is not researched adequately compared to the Voltage Source Inverter (VSI) based systems. A VSI requires a high value of electrolytic capacitor on the dc side and another power conversion/cascaded stage when used in grid connected PV systems (GCPVS) [1]. This increases the complexity and reduces the reliability and efficiency of the overall system. In CSI, on the other hand, single stage power conversion is possible because of its voltage boosting capability. Besides this, improved reliability is achieved as the electrolytic capacitor on the dc side is replaced by an inductor, considering that an electrolytic capacitor is a weak link in any electronic system [2]. Compared to VSI based grid-PV interface, CSI based interface exhibits several advantages that can be summarized as follows:

1) Inherent voltage boost capability, which not only eliminates the need for multiple conversion stages but also enables low voltage PV panels to be used in GCPVS.
2) Draws a continuous dc current from the PV source, which increases the PV life and enhances maximum power point tracking efficiency.
3) The energy storage element is an inductor, which has much longer life time compared to the electrolytic capacitor in VSI.
4) Short circuit protection capability which increases the reliability of the system.

Although CSI has all the above-stated advantages, many challenges need to be addressed when it is used in GCPVS. The main challenge is to reduce the size of the dc link inductor, one of the key elements in CSI, without compromising on the input current ripple. This is because in single phase GCPVS, there is low frequency ripple on the input side that creates low order harmonics in the injected grid current. Apart from this, the input current ripple affects the efficiency of maximum power tracking from the PV array. The typical solution to buffer the ripple power in CSI is to use a high value of input inductor [1]. This high value of inductor on the dc side in the CSI, also needs to carry high current, leading to increased size, cost, losses and poor transient response. Hence, achieving a good quality grid current with a low value of inductor is a challenge, when CSI is used in GCPVS.

Another issue in CSI based GCPVS is the LC resonance caused by the lightly damped CL filter on the ac side. When CSI system is connected to the grid, the grid inductance may vary the LC resonant frequency and this may lead to the excitation of low order harmonics generated either from the SPWM process or from the utility supply [3]. This may increase the distortion in the injected grid current. In order to damp the LC resonance, without degrading the system efficiency, virtual resistance damping is implemented in this work, which is preferred over the passive damping methods.

In transformer-less GCPVS, there exists a path for the ground leakage current due to the grounding of the PV terminals and the grid neutral, irrespective of whether it is a CSI or a VSI. If transformer is used, then the path for the leakage current is mainly through the parasitic capacitance of the transformer. As the value of such capacitance is too low (in the order of pico Farad), the impedance of the path is high and the magnitude of leakage current is greatly reduced. But in transformer-less GCPVS, the leakage current has significant value, which in turn causes adverse effects [4,5]. Therefore, an effective attenuation of the ground leakage current needs to be accomplished in CSI based transformer-less grid-PV interface.

Compared to the VSI, single phase CSI with single stage power conversion has been investigated to a much lesser extent for transformer-less grid connected PV systems at the distribution level. In [1], a double tuned parallel resonant circuit in series with the input inductor is used to reduce the current ripple on the dc side. Further, a modified modulation technique is proposed to reduce the switching frequency

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harmonics in the ac side current. In single stage conventional CSI reported in [6], the double frequency component is extracted from the input current and a nonlinear modulation technique is proposed to improve the quality of the grid current. Though this method reduces the value of the input inductor and improves the grid current quality, it does not address the issue of leakage current. A new topology with an additional leg added, similar to the three phase CSI structure with one of the legs connected to the grid through a capacitor, is proposed in [7]. Here, the current through the capacitor is controlled to reduce the ripple on the dc side. A new CSI with a power decoupling circuit known as active buffer is suggested in [8], where decoupling is done by a small film capacitor. However, extensive computations are needed for the modulation technique.

Modification in the carrier wave using the concept of pulse area modulation, proposed in [9], offers improvement in the quality of the grid current by reducing the lower order harmonics. The method is cost effective and simple to implement but only open loop results are discussed in the paper. In [10], a dual transformer-less topology with single stage power converter is proposed and experimentally verified for two different renewable sources like PV and fuel cell. An intelligent energy management strategy is suggested in the paper for improving the efficiency and reliability. All these methods are suitable for single phase transformer-less grid connected systems with respect to low frequency ripple reduction and voltage boosting capability. However, none of these papers address the leakage current problem, which is considered as one of the major issues in a transformer-less PV-grid interface. The CSI topology reported in [11], reduces the ground leakage current but at the cost of increased number of switches. Besides this, the experimental verification is done at a low power level.

In this work, the conventional single phase CSI structure is modified without increasing the number of semiconductor switches to eliminate the leakage current and make it suitable for transformer-less GCPVS. A modification in the control scheme is proposed for reducing the value of the input inductor and also to compensate the deviation in the LC resonant frequency, maintaining high quality output current. The proposed modification in the structure and in the control scheme is able to achieve several goals such as input current ripple reduction, virtual resistance damping and reference current tracking for a laboratory prototype of 250W power level. All simulation and experimental results are presented to validate the theoretical claims, thereby proving CSI can be used as an interlink between the DG and the utility grid.

II. MODIFIED CSI STRUCTURE AND LEAKAGE CURRENT

Fig. 1(a) depicts the conventional structure of a CSI with C_{pv} as the parasitic capacitance of the PV panel. The parasitic capacitance varies depending on the type of PV panel, atmospheric conditions, power level, dust on the panel etc. Value of C_{pv} is estimated to be 50-150nF/kW for crystalline silicon modules and 1μF/kW for thin film modules [12].

Switching pattern of the conventional CSI is shown in Table I. In the conventional CSI, as presented in Fig.1(c) and Fig.1(d), only two modes of operation in the positive half cycle of the ac side voltage are presented as the operation is symmetrical. It is observed from Fig.1(c) and Fig.1(d) that the common mode voltage (V_{cm}) varies at the switching frequency with the value equal to the voltage across the output filter capacitor (V_{cf}). This results in voltage variation across C_{pv} and generates high ground leakage current. Hence, the conventional CSI structure needs to be restructured or modified to reduce the leakage current, when used for transformer-less grid interface.

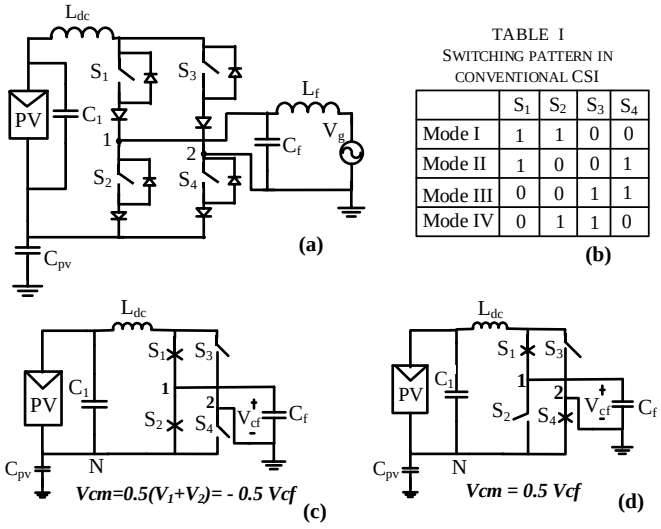

TABLE I
SWITCHING PATTERN IN CONVENTIONAL CSI

	S_1	S_2	S_3	S_4
Mode I	1	1	0	0
Mode II	1	0	0	1
Mode III	0	0	1	1
Mode IV	0	1	1	0

(b)

Fig. 1. Conventional CSI (a) Structure; (b) Switching pattern;(c) Mode I- Charging of L_{dc} and (d) Mode II- Discharging of L_{dc}.

In this work, the conventional CSI is modified as shown in Fig. 2, by adding a split capacitor across the input source and connecting the midpoint of the split capacitor to the grid neutral. In addition to this, the dc link inductor (L_{dc}) is replaced by a common mode choke which is placed in the forward and return paths of the input current [13]. These modifications reduce the ground leakage current as well as the electromagnetic interference.

The switching sequence is also modified as shown in Table II, to reduce the switching losses. As seen in Fig. 2(a), L_{dc} is charged in Mode I, when S_1 and S_2 are switched ON. During the charging of L_{dc}, S_4 is kept ON. This helps in reducing the switching losses without increasing the conduction losses in S_4, because there is no current flow in S_4. The operation of switches in Mode II are similar to that of the conventional CSI. For ease of analysis, only positive half cycle of grid voltage is considered. A symmetrical operation takes place in the negative half of the grid voltage in Mode III and Mode IV.

In this modified CSI structure, the voltage across the parasitic capacitance C_{pv} is clamped and therefore leakage current is negligible. Selection of various parameters for the modified CSI structure is discussed in the following subsections.

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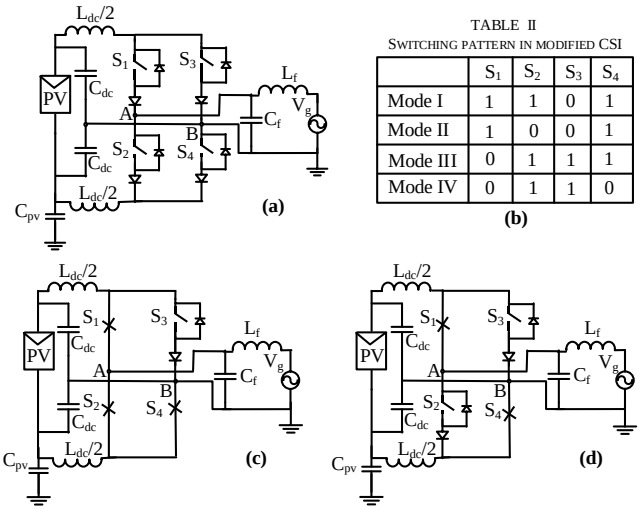

TABLE II
SWITCHING PATTERN IN MODIFIED CSI

	S_1	S_2	S_3	S_4
Mode I	1	1	0	1
Mode II	1	0	0	1
Mode III	0	1	1	1
Mode IV	0	1	1	0

Fig. 2. (a) Proposed modified CSI structure for the transformer-less grid – PV interface: (b) Switching pattern; (c) Mode I-Charging of L_{dc} and (d) Mode II-Discharging of L_{dc}.

A. Selection of input voltage (V_{in})

In a VSI, in the grid connected mode, the input voltage needs to be higher than the peak of the grid voltage. A similar relation for CSI is derived in this subsection. Considering unity power factor (upf) and assuming a lossless inverter, the input dc power is equated to the average output power as follows:

$$V_{in} \times I_{in} = \frac{V_{g\,max} \times I_{g\,max}}{2} \tag{1}$$

$$\therefore\ V_{in} = \frac{m_a \times V_{g\,max}}{2} \tag{2}$$

Here, m_a is the amplitude modulation index, V_{gmax} and I_{gmax} are the peak values of grid voltage and current, while V_{in} and I_{in} are the input voltage and current. It is clear from (2), that the PV panel voltage should be selected to be lower than half the peak value of grid voltage when m_a is less than unity.

B. Selection of switching frequency (f_s)

In a CSI, the conduction losses are higher and switching losses are lower compared to a VSI of the same power level [14]. Hence, losses in IGBT are compared for both CSI and VSI for the switching frequency ranging from 5kHz to 30kHz as shown in Fig. 3. The two lines in Fig.3 represent losses in the switch in CSI and VSI respectively. Total power loss in the IGBT is found to be comparable at 15kHz marked as the break-even point. Therefore,15kHz is selected as the switching frequency.

C. Selection of input inductor (L_{dc})

The expression for L_{dc}, is derived by considering the double frequency ripple power that needs to be handled by L_{dc}. The detailed derivation is given in [13].

$$L_{dc} = \frac{V_{g\,max} \times I_{g\,max}}{2 \times \omega \times \Delta I_L \times I_{Ldc}} \tag{3}$$

$$i_g(t) = m_a(t) \times (I_{Ldc} + \hat{I}_{Lac} \times \sin 2\omega t) \tag{4}$$

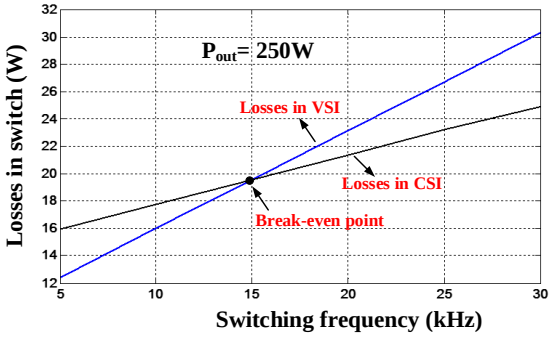

Fig. 3. Variation of losses in the switch with switching frequency.

$$i_g(t) = m_a \times \sin \omega t \times (I_{Ldc} + \hat{I}_{Lac} \times \sin 2\omega t) \tag{5}$$

$$i_g(t) = m_a \times \sin \omega t \times I_{Ldc} + \frac{m_a \times \hat{I}_{Lac}}{2} \times (\cos \omega t - \cos 3\omega t) \tag{6}$$

As seen in (3), L_{dc} depends on the average output power, grid frequency (ω), inductor current (I_{Ldc}) and the peak to peak ripple (ΔI_L) in the inductor current. Obviously a higher value of L_{dc} needs to be selected to reduce the input current ripple as shown in Fig.4(a). This higher value of L_{dc}, not only increases the size, cost and losses but also results in poor transient response.

Neglecting higher order harmonics, the input inductor current ($i_L(t)$), can be written as in (4) and the equation for grid current can be derived as in (6). Here, I_{Ldc} is the average dc current and $\hat{I}_{Lac}$ is the peak value of the second harmonic component in $i_L(t)$. Using trigonometric relations, the magnitude of the third harmonic in the grid current depends on the ripple in the input current as given in (6). The value of third harmonic component present in the output current for different values of L_{dc} is shown in Fig. 4(b) for 250W output power. Therefore, larger value of L_{dc}, reduces the input current ripple and this further reduces the third harmonic content in the output current as shown in Fig. 4(b).

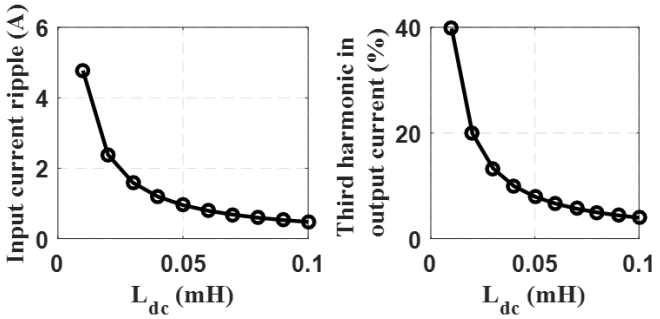

Fig. 4. Variation with input inductor L_{dc}: (a) input current ripple and (b) third harmonic in the output current.

For the conventional control method, from (3), L_{dc} of 100mH needs to be used for a peak to peak second harmonic current ripple of 0.64A at 250W output power for 40V input dc voltage. With the proposed modification in the control

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scheme, which is discussed in the next section, the value of the inductor is reduced to 16mH along with the reduction in the input current ripple.

D. Selection of output filter (C_f and L_f)

The output filter is used to filter mainly the switching frequency components in the output current of the inverter due to SPWM. For selecting the value of C_f, the base impedance (Z_b) of the filter is calculated from the rated power and the grid voltage. Then, the value of the base capacitance is calculated from Z_b. Once C_f is calculated, the value of L_f is obtained based on the resonant frequency [15]. From the frequency response characteristics of the CL filter, for more effective attenuation of switching harmonics, the switching frequency (f_s), should be greater than the resonant frequency. Hence, the resonant frequency is selected as 4000rad/sec. Other parameters are tabulated in Table. III.

TABLE III
SELECTION OF INVERTER PARAMETERS FOR 250W POWER LEVEL

V_{in} (V)	V_{gmax} (V)	L_{dc} (mH)	f_s (kHz)	C_f (μF)	L_f (mH)	C_{dc} (μF)	C_{pv} (nF)
40	100	16	15	6	3	0.22	50

III. MODIFIED MULTI LOOP CONTROL SCHEME

This section discusses the proposed modification in the PWM process, implementation of virtual resistance damping and derivation of the closed loop transfer function for the multi loop control of the proposed CSI based GCPVS.

A. Modification in the SPWM process

In a CSI based GCPVS, the input current is higher than the output current and this makes the input inductor bulky. Also, the inductor value needs to be higher to handle the double frequency ripple power, when it is connected to the single phase grid. In order to make the CSI based GCPVS smaller and compact, economical and efficient, the input inductor value needs to be reduced. However, the reduction in the value of inductor increases the ripple in the input current, thereby increasing the lower order harmonics (LOH) in the output current as discussed in the previous section. A modification in the SPWM process is proposed in this work, for the ripple reduction in the input current without undermining the quality of grid current. The unity peak carrier wave (I_{tpeak}) is multiplied with the instantaneous inductor current $i_L(t)$ as shown in Fig. 5(a) and the equation for the modified carrier wave $\hat{I}_{tri}(t)$ is obtained as below:

$$\hat{I}_{tri}(t) = I_{tpeak} \times i_L(t) = (I_{Ldc} + \hat{I}_{Lac} \times \sin 2\omega t) \qquad (7)$$

After multiplication, the peak of the triangular wave varies with a second harmonic envelop as presented in Fig. 5(b). The modified carrier wave is then compared with the sinusoidal modulating wave to generate the pulses. When the input current increases, peak of the carrier increases, thereby decreasing the pulse width. Hence, the output current and the output power decreases, with a corresponding decrease in the input current. This reduces the ripple in the input current and therefore, a lower value of inductor can be selected. Besides this, as the ripple in inductor current is reduced, the magnitude of the third harmonic in the grid current is reduced according to the equation (6). This is proved in the simulation study, whose results are presented in the paper.

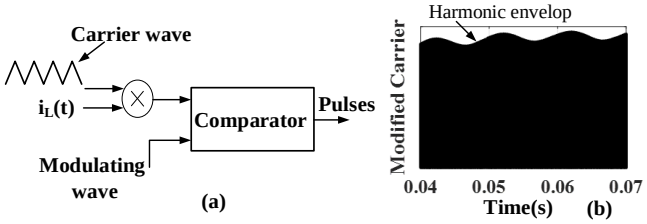

Fig. 5. (a) Proposed modification in the carrier wave and (b) Modified carrier with second harmonic envelop.

However, the aforementioned concept demands modification of the triangular wave by multiplying it with the sensed inductor current $i_L(t)$. For the hardware implementation, DSP processor does not provide the flexibility for such a modification of the triangular wave. Alternatively, during the experimental work, in order to produce the same result, an additional sinusoidal modulating signal (m_{a2}) is generated by dividing the unit amplitude sine wave obtained from the PLL (used for synchronization with the grid) by the sensed current $i_L(t)$ as illustrated in Fig. 6. Therefore, two modulating signals are generated, one for the input current ripple reduction (m_{a2}) and another one for the tracking of the reference current (m_{a1}).

The final modulating signal (m_a) obtained, after adding m_{a1} with m_{a2}, is compared with the conventional triangular wave in the SPWM process. The method is simple and cost effective, because no additional current sensing and no extra hardware is needed for this method. Sensed inductor current is needed but the input current sensing is already done for the maximum power point tracking (MPPT) of the PV array. This low cost ripple reduction method permits the use of low value of input inductor. Therefore, this method offers a good solution to the major challenge faced by single phase CSI based GCPVS.

B. Virtual Resistance damping (VRD)

When CSI is interfaced with the grid through a CL filter, the increase in the inductance attenuates the resonant frequency of the CL filter and causes low order harmonic resonance. This resonance distorts the CSI output current and hence damping is essential to improve the quality of the output current. The damping can be incorporated by connecting physical resistor either across the output filter capacitor or in series with the filter inductor in CSI based GCPVS [16-18]. However, this increases the power losses in the system, as the grid frequency current flows through the damping resistor. Hence, VRD is implemented in this work, to provide the damping without degrading the efficiency.

VRD is implemented through a feedback loop without

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connecting a real resistor in the system. The damping current I_{damp}, is calculated by filtering the voltage across the output filter capacitor (V_{cf}) and dividing by the damping resistance (R_d) as given in Fig. 6. High pass filter is used for filtering V_{cf}, in order to extract the harmonic component of the capacitor voltage, without affecting the current control at the fundamental frequency [3]. There is a trade off in selecting the value of R_d, which is discussed in detail in the next section.

C. Analysis of the multi loop control

Multi loop control consists of an outer current control loop and an inner voltage control loop as depicted in Fig.6. Controller tuning in multi loop control is an interactive process, as the controller gain of the outer current control loop affects the voltage controller gain of the inner loop for a specified value of band width and steady state error (SSE). Output filter capacitor voltage (V_{cf}) is the control variable chosen for the inner loop because it directly senses the disturbance in grid voltage.

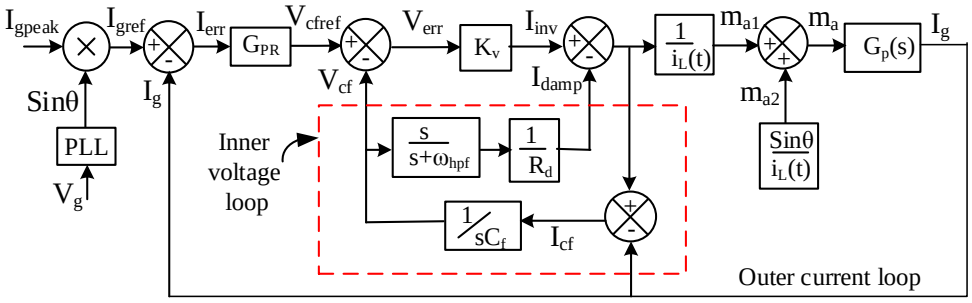

Fig. 6. Proposed control scheme with outer current and inner voltage loop.

The inner loop uses a proportional controller of gain K_v, as the SSE in the capacitor voltage, does not affect the performance of the outer current control loop [19]. Considering the inner voltage control loop, G_{Vcfref}, which is the ratio of the grid current (I_g) and the reference capacitor voltage (V_{cfref}) is derived as given below, by applying block diagram reduction rules in Fig. 6.

$$G_{V_{cfref}} = \frac{K_v(s+\omega_{hpf})}{s^3 L_f C_f + s^2\left(L_f C_f \omega_{hpf} + \frac{L_f}{R_d} + K_v L_f\right) + s(K_v L_f \omega_{hpf} + 1) + \omega_{hpf}} \quad (8)$$

For tracking the current reference with negligible SSE in the outer current control loop, a Proportional Resonant (PR) controller with a transfer function, G_{PR} is used. Compared to a PI controller in synchronous frame, PR controller is selected to reduce the computational burden [20]. Thus, the open loop transfer function $G_i(ol)$, can be obtained as given below:

$$G_i(ol) = G_{PR} \times G_{Vcfref} \; ; \; G_{PR} = K_p + \frac{K_i \times \omega_{cut} s}{s^2 + 2\omega_{cut} s + \omega_o^2} \quad (9)$$

A detailed study is carried out on the dynamic response of the virtual damping current control loop. Control block diagram of the virtual resistance damping loop is shown in Fig. 7, where ω_{hpf} is the cut off frequency of the high pass filter. As seen from Fig. 7, there are two inputs for the damping loop such as the output current of the inverter (I_{inv}) and the grid voltage (V_g). By applying superposition theorem and block diagram reduction, the ratio of I_{damp} to I_{inv} (G_{ii}), and I_{damp} to V_g (G_{iv}) are found out as given below:

$$G_{ii} = \frac{s^2 L_f}{s^3 L_f R_d C_f + s^2\left(L_f C_f R_d \omega_{hpf} + L_f\right) + sR_d + \omega_{hpf} R_d} \quad (10)$$

$$G_{iv} = \frac{s}{s^3 L_f R_d C_f + s^2\left(L_f C_f R_d \omega_{hpf} + L_f\right) + sR_d + \omega_{hpf} R_d} \quad (11)$$

Step response of the damping loop for the transfer functions given in (10) and (11) is shown in Fig. 8(a) and Fig. 8(b) respectively, for different values of the virtual resistance R_d. In both cases, a larger value of R_d reduces the overshoot of I_{damp}, but increases the oscillation settling time, as seen in Fig. 8. This is expected as R_d is considered to be connected in parallel with the capacitor C_f. If the settling time of I_{damp} is longer, the system damping with that value of R_d is less effective. Hence, there is a trade off in selecting R_d.

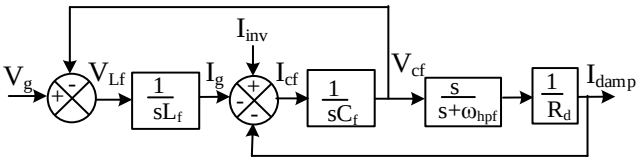

Fig.7. Control block diagram of the virtual resistance damping loop.

Next, the design of the PR controller is discussed. Controller gains of the PR controller are obtained from the open loop gain of the system $G_i(ol)$ given in (9), by selecting a suitable value for bandwidth and the cut off frequency ω_{cut}. Two equations are obtained from (9), one at the grid frequency to meet the SSE requirement and another at the bandwidth frequency to satisfy the bandwidth requirement. By solving these two equations, the controller gains (K_p and K_i) of G_{PR}, as given in Table IV, can be determined. The transfer function obtained is given below:

$$G_{PR} = \frac{0.58s^2 + 212.35s + 57240.33}{s^2 + 1.256s + 98690} \quad (12)$$

The Bode plot of the G_{Vcfref} and open loop gain $G_i(ol)$ is shown in Fig. 9(a). It is observed that the gain at grid

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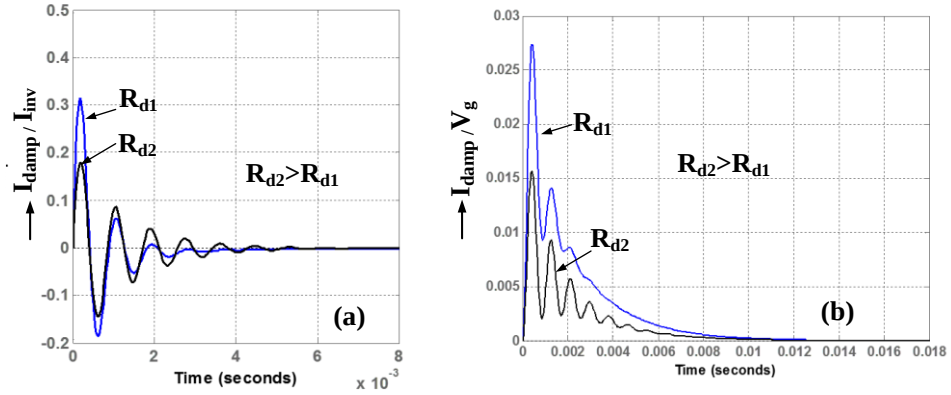

Fig. 8. Step response of the damping loop: (a) ratio of I_{damp} and I_{inv} and (b) ratio of I_{damp} and V_g.

frequency of 50Hz (314rad/sec) is 64dB, which corresponds to a SSE of less than 1%. Therefore, the designed PR controller can effectively track the reference. Besides this, frequency response analysis of the loop gain is carried out by varying the value of the proportional controller (K_v) and damping resistance (R_d). The corresponding Bode plots are presented in Fig. 9(b) and Fig. 9(c).

The effect of the variation in the voltage controller gain, K_v on the open loop system is shown in Fig. 9(b). Higher value of K_v leads to a more effectively damped system. However, with the increase in K_v, it is seen that the gain at low frequency increases and this leads to the increase of low frequency noise thereby affecting the system stability [3]. Higher value of K_v, also introduces a phase shift at grid frequency as seen in Fig. 9(b). The outer current control loop should compensate for this phase shift, to minimize the SSE in the reference current tracking. Hence, the value of K_v is finalized based on the simulation study and the value used in simulation and experimentation is given in Table IV.

TABLE IV
VALUES SELECTED FOR MULTI LOOP CONTROL

K_v	ω_{hpf} rad/sec	R_d Ω	K_p	K_i	ω_{cut} rad/sec	K_{ppll}	K_{ipll}
2	440	50	0.58	373	0.628	0.56	26

It is observed from Fig. 9(c) that, as the value of R_d is increased, the phase margin is increased and this improves the dynamics of the damping loop. A small value of R_d reduces the distortion in the output current but makes the inverter system unstable [3]. The value of R_d is finalized from this analysis, from the step response of the damping loop and from the simulation study and given in Table IV.

PLL is implemented using inverse park transformation with the gains of the PI controller (K_{ppll} and K_{ipll}) as given in Table IV, following the procedure given in [21] and maximum power point is tracked using the conventional Incremental Conductance Algorithm.

IV. Simulation and Experimental Results

The proposed CSI topology and the multi loop control is validated through simulation and experiments. The results are discussed in this section.

A. Simulation Results

Simulation is carried out for the CSI based GCPVS with the modified CSI structure with the proposed modification in the control. The system parameters are chosen as given in Table. III for the simulation. Fig.10(a) and Fig.10(b) presents the variation in the input current ripple and the inverter output current with conventional carrier and with the modified carrier wave in the stand-alone mode. Noticeable reduction in

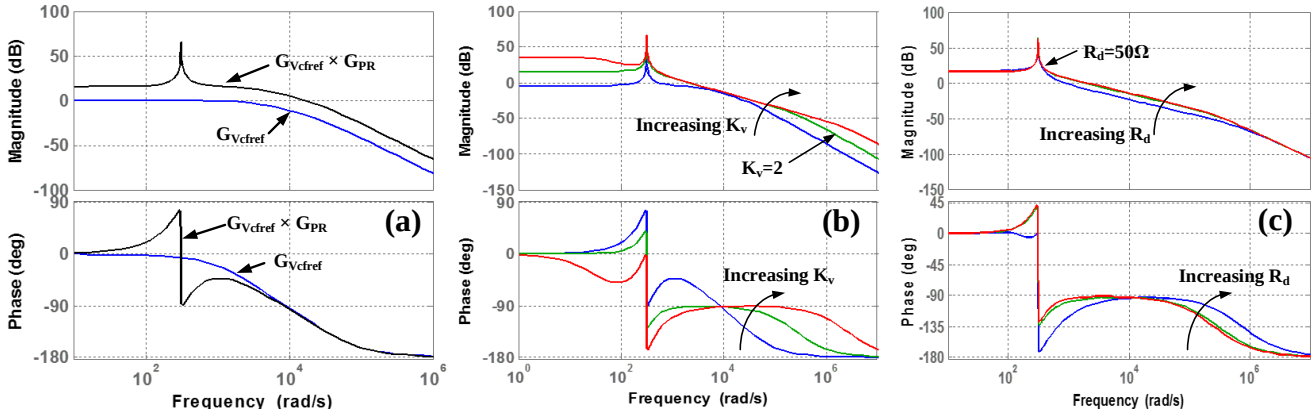

Fig .9. (a) Bode plots of G_{Vcfref} and loop gain (G_{Vcfref} × G_{PR}) (b) Effect of varying K_v and (c) Effect of varying R_d, on the loop gain.

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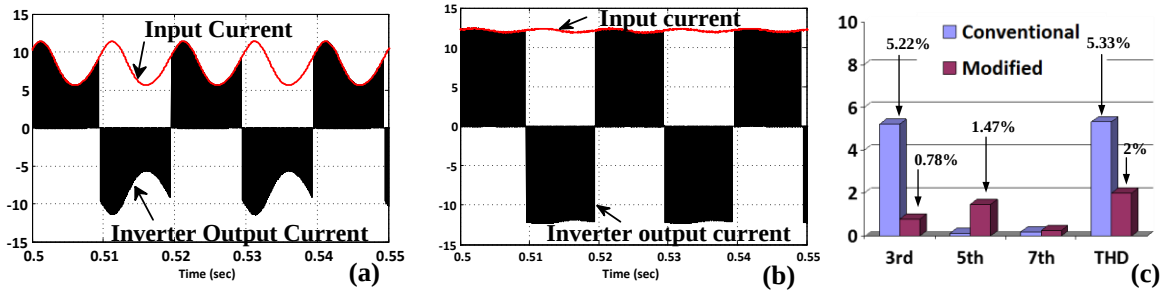

Fig. 10. Simulated waveforms: (a) with conventional carrier; (b) with modified carrier and (c) Harmonic Spectrum of output current.

the current ripple is obtained. This improves the quality of output current fed in to the grid, because the current ripple, processed by the SPWM process is less. Furthermore, the inductor value is also reduced, which not only reduces the cost and size of the overall system but also improves the efficiency and transient response of the system. Harmonic spectrum of the output current shown in Fig.10(c) proved the theoretical claim that the third harmonics and the THD are reduced with the proposed modification in the carrier wave. THD is reduced from 5.33% to 2% with the proposed method.

Method used in the experimental work (as discussed in Section III.A), is also verified in the simulation. PV model is used as the input source. To verify the effectiveness of the PR controller, the irradiation level is changed from 800W/m^2 to 1000W/m^2 at 1sec. The resultant modulating signal (m_a), after the addition of m_{a1} and m_{a2}, which is used for comparison with the conventional carrier wave is shown in Fig. 11(a). Leakage current is measured in simulation as well as during experimentation by connecting a capacitor (C_{pv}) of value 22nF, emulating the parasitic capacitance of the PV array. Insignificant leakage current is observed as shown in Fig. 11(b). Hence, the proposed modification in the CSI structure fulfills the requirement of low leakage current.

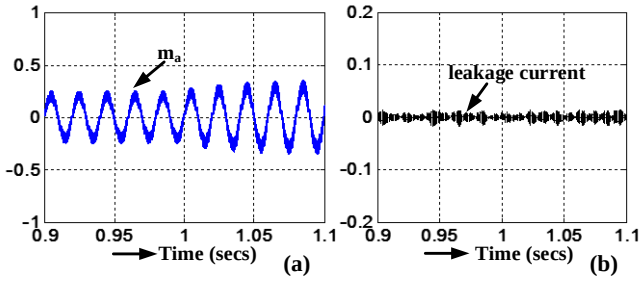

Fig. 11. (a) Modulating signal and (b) Leakage current.

With the change in irradiation, the damping current I_{damp}, that contains only harmonic current components is shown in Fig. 12(a). Corresponding increase is observed in the reference current, followed by increase in the grid current as portrayed in Fig. 12(b). Hence it is verified that the PR controller tracks the reference current. Besides this, it is clear from the simulation results that, the distortion in the grid current is well within the specified limits using the multi loop control. Also, the value of the input inductor (L_{dc}), is reduced from 100mH to 16mH as compared to the conventional control method.

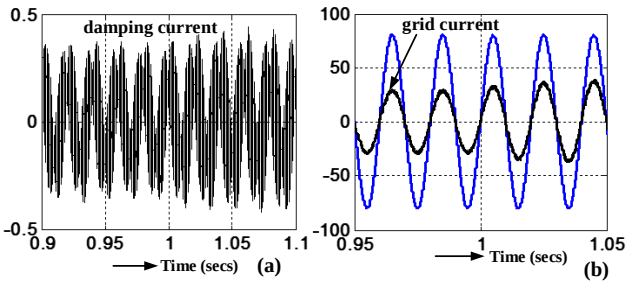

Fig. 12. (a) damping current and (b) Grid voltage and current (1:10).

B. Experimental Results

The system parameters used for the simulation study (Table III), are also used for the implementation of 250W laboratory prototype. DSP controller TMS320F28335 is used for the control. Photograph of the experimental setup is depicted in Fig. 13.

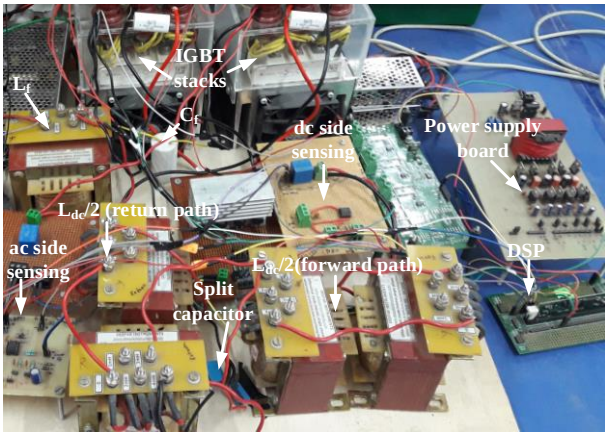

Fig. 13. Photo of the experimental set up.

Two inductors of value 8mH each are used in the forward path and return paths of the dc side current. PV emulator Terra SAS Amtek (600V, 8A, 5.8kW) is used as the PV source and semikron IGBT stacks are used for the CSI structure. Two LEM sensors, LA25-P and HX-05-P are used for dc side and ac side current sensing respectively. Split capacitor arrangement is used across the input and the midpoint is connected to the neutral of the single phase grid.

Fig. 14(a) represents the input voltage of the PV emulator for 224W (36.24V, 6.16A) input power. Fig. 14(b) shows a

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screen shot of the P-V and I-V characteristics from the PV emulator and MPPT from PV, for the same input voltage and current. Around 95% MPPT efficiency is achieved at this power level.

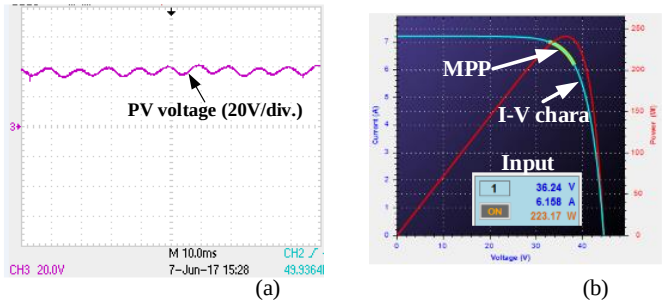

Fig.14. Experimental waveforms in grid connected mode: (a) PV voltage and (b) Maximum Power Point Tracking (from PV emulator).

In order to prove the reduction in the current ripple, the input current is measured in open loop and closed loop for the same operating conditions. The open loop current waveform presented in Fig. 15(a), shows a peak to peak current ripple of 5A of double the grid frequency (100Hz). This 100Hz ripple is present in the inverter output current as seen in Fig. 15(b), which contributes to the increase in the distortion in the injected grid current. Fig.15(c) depicts the input current in closed loop with a peak to peak ripple of around 0.2A. Significant reduction in the peak to peak current ripple is achieved in closed loop because of the proposed modification in the control loop.

The system is connected to the grid through an autotransformer through a contactor. Grid voltage and injected current waveforms for 200W of active power injection are shown in Fig. 15(d). Measured THD of the injected current is 4.78%, which satisfies the IEEE standards [22,23]. An efficiency of around 88% is achieved at this power level.

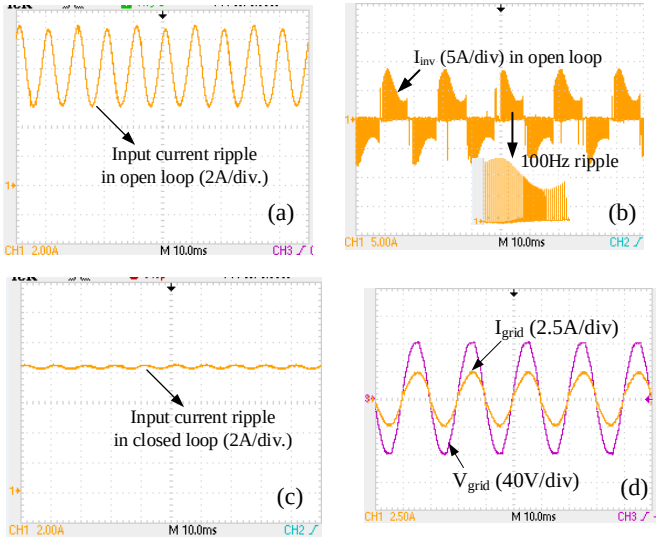

Fig. 15. Experimental waveforms: (a) Input current in open loop (b) Inverter output current in open loop; (c) Input current in closed loop and (d) Grid voltage and grid current.

All current waveforms are measured using the Tektronix TCPA 300 current probe. Grid voltage and current for another value of power injection (120W power), in to the grid and the corresponding THD in the output current are shown in Fig. 16(a) and Fig.16(b) respectively.

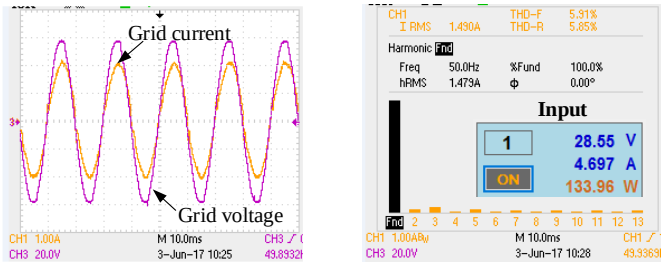

Fig. 16. (a) Grid voltage and current for 120W power injection and (b) THD.

For measuring the efficiency of the CSI system, the PV emulator is replaced by a dc input source (60V,25A Lamda supply) and the grid is replaced by a resistive load of 80Ω. Efficiency is plotted for different values of input power and is presented in Fig. 17(a). Around 89% efficiency is obtained at the rated power for the laboratory prototype. Leakage current measurement is carried out in a similar way as that of the simulation, using the capacitor arrangement. Insignificant leakage current is observed as portrayed in Fig. 17(b). A brief comparison of the CSI topologies is given in Table V.

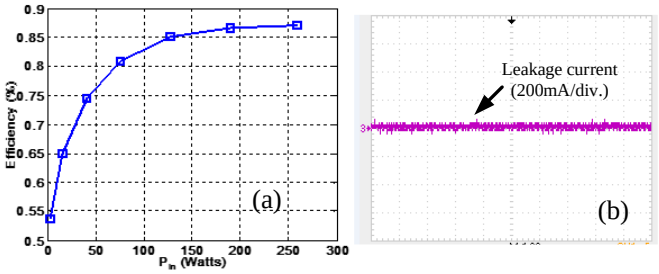

Fig.17. (a) Efficiency versus input power and (b) Measured leakage current.

V. CONCLUSION

A single phase single stage CSI that can meet the requirements of transformer-less grid connected PV system is proposed, analyzed and experimentally validated in this paper. Modification in the multi loop control is proposed and implemented, that not only reduces the input current ripple, but also enables the use of a smaller inductor on the dc side. Furthermore, virtual damping is provided in the control loop to compensate the effect of variation in the LC resonance without degrading the efficiency. The proposed CSI system is able to achieve the following objectives in addition to the usual advantages of a conventional CSI:

(1) Negligible ground leakage current without increasing the switch count.

(2) Significant reduction in the value of input inductor without compromising on the input current ripple.

(3) Tracking of the reference current with very small steady state error.

(4) Injecting good quality, upf current in to the utility grid.

TABLE V
COMPARISON OF SINGLE PHASE CSI TOPOLOGIES

Parameters	[1]	[6]	[8]	[11]	[24]	Proposed
No. of components (S-D-L-C)	4-0-4-3	4-0-2-2	5-2-2-3	7-1-2-2	5-1-2-2	4-0-2-3
THD	2.73%	4.42%	4.24%	***	***	4.78%
Rated Power	500W	1000W	400W	Less than 50W	500W	250W
Leakage current	***	***	***	Negligible	***	Negligible

S=switch; D=diode; L=inductor; C=capacitor; *** not reported

(5) Virtual resistance damping to reduce current distortion.

Experimental results show that the input current ripple is significantly reduced, in addition to the 84% reduction in the input inductor value for the 250W power level. The output current THD of less than 5% is observed for 200W of active power injection, with negligible leakage current. Therefore, it is verified experimentally and in the simulation study that multiple objectives are achieved with the proposed modifications in the CSI structure and in the control. Hence, the modified CSI structure with the proposed modification in the multi loop control is promising for single phase, single stage transformer-less grid-PV interface applications.

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