Robust Deadbeat Control Scheme for a Hybrid APF With Resetting Filter and ADALINE-Based Harmonic Estimation Algorithm

Yang Han, *Member, IEEE*, Lin Xu, Muhammad Mansoor Khan, Chen Chen, *Senior Member, IEEE*, Gang Yao, and Li-Dan Zhou

***Abstract*—A novel hybrid active power filter (HAPF) topology is proposed, which shows advantages of the conventional HAPF and the LCL filter in terms of reduced dc-link voltage, lower switching ripples, and less electromagnetic interference injection. To enhance the noise rejection capability of the digital controller, the resetting filters (RFs) are utilized as prefilters before the analog/digital sampling stage. A robust deadbeat current control law is derived based on the average current tracking scheme, where the effect of the RFs is favorably incorporated. To alleviate the difficulties in current controller design, the ac-side capacitor voltage of the HAPF is estimated by using the adaptive linear neural network identifier in the load current feedforward loop. Hence, a simple proportional controller is utilized in the inner current loop. Moreover, the grid current feedback and load current feedforward strategies are used to achieve precise current tracking and fast dynamic response. A 75-kVA prototype system is built for verification. The validity of the proposed HAPF and its control algorithms are confirmed by the experimental results.**

***Index Terms*—Active power filters (APFs), adaptive linear neural network (ADALINE), harmonic contamination, LCL filter, power quality, resetting filter (RF).**

I. Introduction

ELECTRICAL power quality has been an important and growing problem due to the proliferation of the nonlinear loads, which causes a significant increase in the line losses, instability, and voltage distortions [1]–[3]. This fact has led to the proposal of more strict requirements regarding power quality like those specifically collected in the standards IEC-61000-3-{2,4} and IEEE-519 [4], [5]. In recent decades, active power filters (APFs) have been recognized as the most effective solutions for harmonic mitigation. A lot of the recent literature investigate and try to improve APFs by developing new topologies or new control algorithms [1]–[3], [6]–[8], [10]–[25].

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In retrospect, it was reported in the previous literature [9]–[13] that the performance of APFs is highly dependent on how the reference signals are generated. The instantaneous reactive power theory approach [9]–[14], the efficient discrete Fourier transformation [15], the Fortescue decomposition method [16], and the adaptive linear neural networks (NNs) (ADALINEs) [17]–[19] were extensively investigated for reference current generation (RCG) purposes for the APFs. Recently, the genetic algorithm (GA) [20] has been utilized for the APFs, which shows drawbacks concerning the global stability of the closed-loop system. To overcome the shortcomings of the GA, more advanced techniques have been proposed in the literature, including the sliding-mode control [21], adaptive notch filter approach [22], and direct power control [23]. To achieve low harmonic distortion, the repetitive controller [24] and the resonant compensators [25] were utilized for harmonic compensation. In [6], the deadbeat control scheme was reported, which offers the potential for the fastest transient response and full compatibility with the digital platforms.

In addition to the RCG schemes and the current control strategies, the switching ripple attenuation and electromagnetic interference (EMI) reduction are also crucial for the practical implementation of the APFs. To resolve the issues of the switching ripple and EMI reduction, normally, a big value inductance for output filtering must be adopted [13], which degrades system dynamics. By connecting a small-rated APF to the single-tuned LC filter to form the hybrid topology, the dc-link voltage of the voltage source inverter (VSI) can be reduced to a fraction of the main voltages [1], [13], [17], [26]–[28].

To take advantage of the hybrid LC-filter topology for reduced dc-link voltage and the LCL filter for better switching ripple attenuation, a novel hybrid APF (HAPF) is presented in this paper. By using the third-order LCL filter to replace the L section of the resonant LC filter, the total filter inductors are remarkably reduced, and perfect switching ripple attenuation is achieved. To eliminate the effects of switching noise on the performance of current tracking, the resetting filters (RFs) are implemented as prefilters [27]. The preliminary result of this HAPF was presented in [28]. However, the effect of RFs, the robustness of the current controller, and the ac-side capacitor voltage estimation method were not discussed in [28]. This paper aims to clarify the misunderstanding in [28] and provides the detailed elaboration on the control algorithms. Instead of using the instantaneous current tracking, the average current

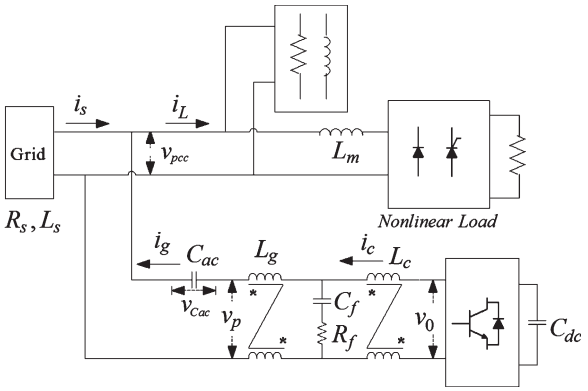

Fig. 1. Single-phase schematic of the proposed hybrid LCL-filter-based APF.

control scheme is derived, where the effect of the RFs is incorporated. A novel scheme for the ac-side capacitor voltage estimation is proposed, using the ADALINE identifier [17]–[19] in the feedforward loop, which simplifies the controller design and achieves selective harmonic compensation purposes.

This paper is organized as follows. The mathematical model of the proposed HAPF is presented in Section II. The controller synthesis methodologies of the HAPF are presented in Section III, which includes the elaboration on the RFs, the ADALINE identification scheme, the ac-side capacitor voltage estimation method, and the feedforward plus feedback control strategies. The experimental results are presented in Sections IV. Finally, Section V concludes this paper.

II. Mathematical Modeling of the Proposed Hybrid LCL-APF

Fig. 1 shows the circuit diagram of the proposed LCL-filter-based HAPF. Three single-phase topologies are utilized in the prototype system as demonstrated by the experimental results; thus, only a single-phase representation is illustrated. The LCL filter, which consists of L_g, C_f, and L_c with possible passive damping resistance R_f, is used as the output filter of the VSI and grid interface. The damping resistors would introduce additional power loss; to overcome the drawback, the active damping for the LCL resonance was applied in pulsewidth modulation (PWM) rectifiers in [26]. However, in the case of the LCL-filter-based APFs, the active damping complicates the controller design and requires more current sensors, which increase the cost of the digital controllers. Hence, the passive damping scheme is considered in this paper.

The LCL section is equivalent to an inductor (L filter) at lower frequencies. Hence, the LC resonant topology is formed between the LCL filter and ac-side capacitor $C_{\rm ac}$ in the low-frequency range; thus, the dc-link voltage of the VSI is remarkably reduced to achieve lower EMI emission and higher inverter efficiency. Referring to Fig. 1, the system equations can be easily derived according to Kirchhoff's laws, which yield

$$\begin{cases} L_g \frac{di_g}{dt} = R_f(i_c - i_g) + v_{\rm cf} + v_{\rm Cac} - v_{\rm pcc} \\ L_c \frac{di_c}{dt} = -R_f(i_c - i_g) - v_{\rm cf} + v_o \\ C_{\rm ac} \frac{dv_{\rm Cac}}{dt} = -i_g \\ C_f \frac{dv_{\rm cf}}{dt} = i_c - i_g \end{cases} \tag{1}$$

TABLE I
Specifications and System Parameters

Name	Parameters
APF power rating	75 kVA (3-phase)
Nominal grid voltage (phase-to-phase)	380 V(RMS)
Ac-side capacitor C_{ac}	1000 μF
Grid-side inductor of the LCL-filter $L_{\rm g}$	250 μH
Converter-side inductor of the LCL-filter $L_{\rm c}$	500 μH
Ac capacitor of the LCL-filter C_f	10 μF
Damping resistance R_f	2 Ω
Dc-side voltage of the VSI	300 V
A/D sampling frequency	10 kHz
Inverter switching frequency	10 kHz

where parameters i_g and i_c are the inverter currents across the inductors L_g and L_c, respectively, i_f and $v_{\rm cf}$ represent the current and voltage across the capacitor of the RC-filter branch, and $v_{\rm Cac}$ is the voltage across the ac-side capacitor $C_{\rm ac}$. Let $L_g = L_{g0} + \Delta L_g$, $L_c = L_{c0} + \Delta L_c$, $C_{\rm ac} = C_{\rm ac0} + \Delta C_{\rm ac}$, $C_f = C_{f0} + \Delta C_f$, and $R_f = R_{f0} + \Delta R_f$, where the subscript "0" denotes the nominal value; L_{g0}, L_{c0}, $C_{\rm ac0}$, C_{f0}, and R_{f0} are the parameter variations around their nominal values. Rearranging (1), we define

$$\begin{cases} f_1 = \Delta R_f(i_c - i_g) - \Delta L_g \frac{di_g}{dt} - v_{\rm pcc} + n_1 \\ f_2 = \Delta R_f(i_g - i_c) - \Delta L_c \frac{di_c}{dt} + n_2 \\ f_3 = -\Delta C_{\rm ac} \frac{dv_{\rm Cac}}{dt} + n_3 \\ f_4 = -\Delta C_f \frac{dv_{\rm cf}}{dt} + n_4 \end{cases} \tag{2}$$

where n_1, n_2, n_3, and n_4 represent unstructured uncertainties due to unmodeled dynamics. From (1) and (2), we get

$$\dot{\mathbf{x}} = \mathbf{A_{c0}}\mathbf{x} + \mathbf{B_{c0}}\mathbf{u} + \mathbf{G_{c0}}\mathbf{f} \qquad \mathbf{y} = \mathbf{C}\mathbf{x} \tag{3}$$

where the vector of state variables $\mathbf{x} = [i_g, i_c, v_{\rm Cac}, v_{\rm cf}]^T$, the equivalent input vector $\mathbf{u} = [0, v_0, 0, 0]^T$, $\mathbf{f} = [f_1, f_2, f_3, f_4]^T$, and the system matrices $\mathbf{A_{c0}}$, $\mathbf{B_{c0}}$, $\mathbf{G_{c0}}$, and $\mathbf{C}$ are listed in Appendix A.

The major issues regarding the LCL-filter design include the total cost of inductors, the resonant frequency of the hybrid LCL filter, the size of the damping resistance, and the attenuation at the switching frequency to comply with the power quality standards imposed by IEEE 519-1992 and the IEC 61000-3-4 [4], [5]. Under the present case, the resonant frequency at a low-frequency range is selected between the third- and fifth-order harmonic to minimize the total cost of the power stage [28]. The LCL resonant frequency is selected significantly higher than the highest load harmonics compensated by the HAPF, while lower than the Nyquist frequency of the control system [13], [26]. Moreover, the selection of the damping resistance R_f is a compromise between the requirements of the stability margin and power loss limitation. Followed by these guidelines, the specification of the proposed APF is illustrated in [28, Table I].

III. Control System Design

The current control loop is a key element for the APFs [10]–[19]. This section presents the controller synthesis for the proposed HAPF (see Fig. 2). First, the RFs are used as the prefilter for the digital controller, and the ADALINE is utilized

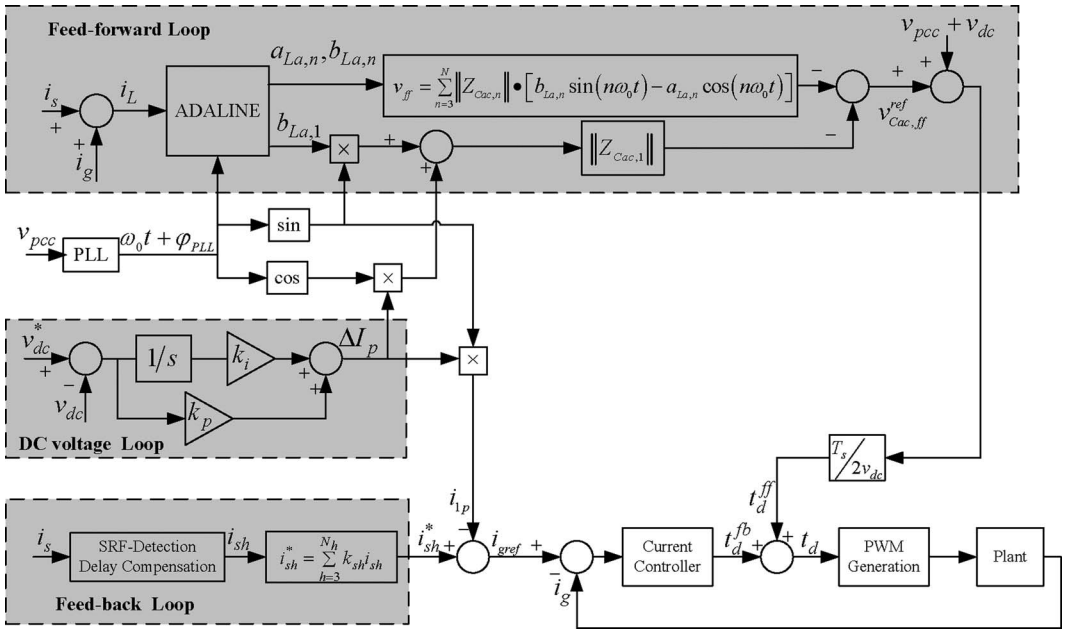

Fig. 2. Control block diagram of the proposed HAPF.

for individual harmonic estimation. The proposed load current feedforward plus grid current feedback scheme is analyzed with emphasis on the average current control law, the ac-side capacitor voltage estimation scheme, the robustness analysis of the current controller, and the stability of the grid current feedback loop. Finally, the dc-link voltage regulation is also discussed.

A. A/D Sampling Using RF

To eliminate the effect of random and switching noise on the performance of the current control scheme, the RFs are utilized as prefilters for the sampling data with excellent noise rejection capability, which is highly desirable for the APF applications.

Fig. 3(a) shows the schematic of the RF, constructed using capacitor $C_{\rm RF}$, resistors $R_{\rm in}$ and $R_{\rm out}$ at the input and output sides of the filter, the operational amplifiers, and the switch array. The capacitor voltage resets to zero at the start of each PWM control cycle. The frequency response of the resetting integrator is derived as [27]

$$G(j\omega) = \frac{1}{j\omega T_s}(1 - e^{-j\omega T_s}). \tag{4}$$

Fig. 3(b) shows the frequency response of the RF with a sampling time $T_s = 100$ μs. It shows that the RF has high rejection of the signals at the harmonics of the switching frequency with the slope of 20 dB/dec. This characteristic is highly appreciated if the sampling is required to be made at other fixed points than the start or middle of the cycle in the case of the constant frequency inverter systems, such as APFs. In case of digital implementation of the APF, one sample delay limits the maximum achievable control bandwidth.

However, if a point other than the start or middle of the control cycle is chosen as the sampling point, the effect of PWM and burr in the current transducer contaminates the signal, and

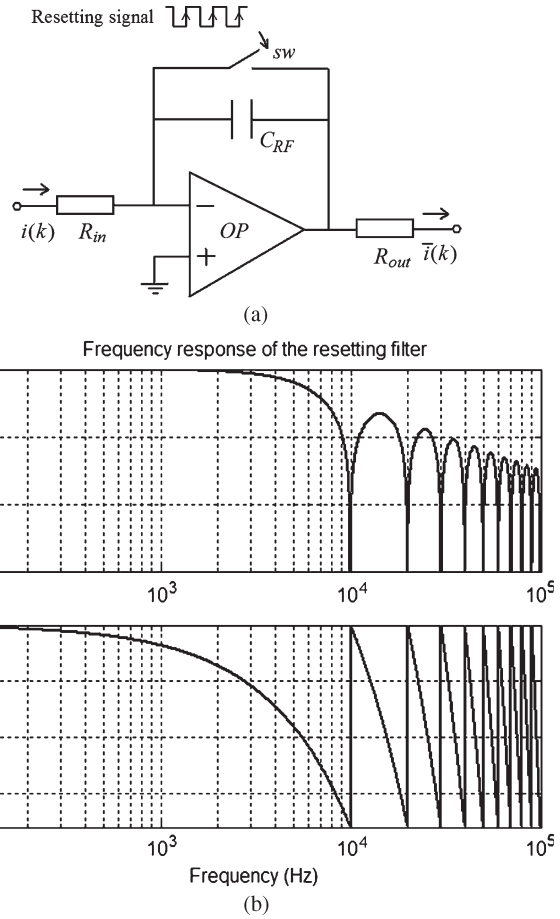

Fig. 3. (a) Schematic of the RF. (b) Frequency response of the RF.

the desired control performance is deteriorated. As these noises are either periodic or limited to the frequencies higher than the switching frequency, the RFs are utilized for noise rejection. Nevertheless, the RFs would modify the system frequency

response and introduce half a cycle delay; this effect would be incorporated in the current loop stability analysis.

B. Harmonic Detection Using the ADALINE

The most critical issues associated with APF control are that of finding an appropriate control algorithm which can obtain an accurate reference signal for control purposes, particularly when the load harmonics are time varying [6]–[8]. To take advantage of online learning capabilities of NNs, the ADALINE is utilized to estimate the time-varying magnitudes and phases of the fundamental and harmonic components from the source current and load current [6]. The motivation of this paper is to achieve the ac-side capacitor voltage estimation to alleviate the current controller design using the load current feedforward loop, which utilizes the ADALINE as harmonic identifiers.

The accuracy and fast-estimation capability of the ADALINE are crucial when selective harmonic mitigation is preferred in current control to reduce the control bandwidth, thus enhancing the system robustness and stability. The guidelines for parameter tuning of the ADALINE algorithm can be found in the previous literature [3], [17]–[19], [29], [30].

C. Proposed Feedback Plus Feedforward Control Strategy

In this section, the feedback plus feedforward control schemes are described, which include the deadbeat control law for the average current control scheme, the ADALINE-based ac-side capacitor voltage estimation method, the stability and robustness analysis of the current controller, etc.

The load current in phase "a" is represented by [17]–[19]

$$\begin{aligned} i_{\mathrm{La}}(t) &= \sum_{n=1}^{\infty} I_{\mathrm{La},n}\sin(n\omega_0 t+\varphi_{\mathrm{La},n}) \\ &= a_{\mathrm{La},1}\sin(\omega_0 t+\varphi_{\mathrm{PLL}})+b_{\mathrm{La},1}\cos(\omega_0 t+\varphi_{\mathrm{PLL}}) \\ &\quad+\sum_{n=2}^{\infty}\left[a_{\mathrm{La},n}\sin(n\omega_0 t)+b_{\mathrm{La},n}\cos(n\omega_0 t)\right] \end{aligned} \tag{5}$$

where $a_{\mathrm{La},1}=I_{\mathrm{La},1}\cos(\varphi_{\mathrm{La},1}-\varphi_{\mathrm{PLL}})$ and $b_{\mathrm{La},1}=I_{\mathrm{La},1}\sin(\varphi_{\mathrm{La},1}-\varphi_{\mathrm{PLL}})$ represent the amplitude of the fundamental active and reactive components of the nonlinear load current and φ_{PLL} represents the initial phase angle of the phase-locked loop (PLL) [28], [29] synchronized with the fundamental component of the grid voltage at the point of common coupling (PCC).

Notably, the grid distortion would have a remarkable effect on the performance of the PLLs, which is why the PLLs are crucial to ensure stable operation of the APFs. Fortunately, however, high-performance PLLs under the grid distortion can be found in [29]. In (5), $I_{\mathrm{La},n}$ and $\varphi_{\mathrm{La},n}$ ($n>1$, where n is an integer) represent the amplitude and phase angle of the nth-order harmonic component of the load current, respectively. The parameters $a_{\mathrm{La},n}$ and $b_{\mathrm{La},n}$ are the weights of the individual harmonic component obtained from the ADALINE algorithm [3], [17]–[19], [21].

1) Derivation of the Average Current Control Law: Utilizing the reduced order model of the LCL section, the differential equation of the inductor current across the LCL filter (i_g) is represented as [28]

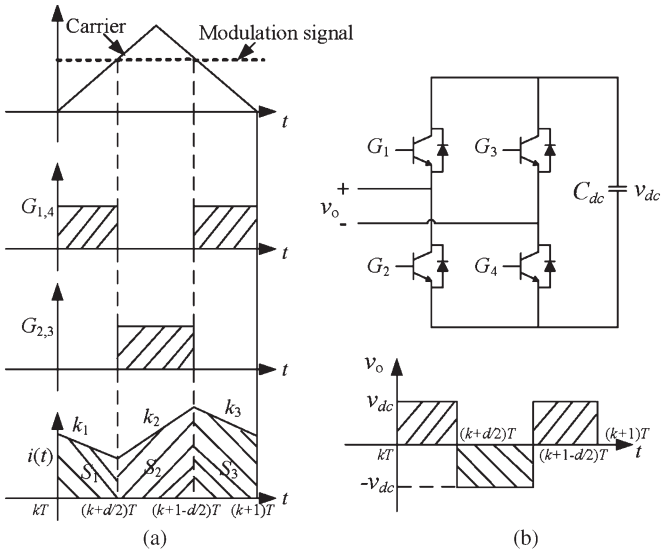

Fig. 4. Principle of current tracking scheme. (a) Geometrical interpretation for deriving the average current during one PWM period. (b) Schematic of the VSI and its output voltage.

$$v_{\mathrm{pcc}}-v_{\mathrm{Cac}}-v_o=-L\frac{di_g}{dt} \tag{6}$$

where parameters v_{pcc}, v_{Cac}, and v_o represent the voltage at the PCC, the ac-capacitor voltage, and the output voltage of the inverter, respectively, and $L=L_g+L_c$. Fig. 4 shows the operation principle of the inverter under different PWM switching patterns.

Therefore, (6) can be rewritten in the discrete form using a piecewise linear representation; hence, the duty ratio of the PWM signal at the kth control period is obtained as [28]

$$\begin{aligned} d[k] &= \frac{L\left\{i_g\left[(k+1)T_s\right]-i_g[kT_s]\right\}}{2v_{\mathrm{dc}}[k]T_s} \\ &\quad+\frac{v_{\mathrm{dc}}[k]+v_{\mathrm{pcc}}[k]-v_{\mathrm{Cac}}[k]}{2v_{\mathrm{dc}}[k]}. \end{aligned} \tag{7}$$

Equation (7) shows that the control signal consists of the feedback error tracking and the ac voltage feedforward term. However, all the sampling signals are the average quantities of the previous control period due to the effect of RFs. Hence, the control law should be modified to account for the average quantities. Note that the duty ratio $d[k]$ is abbreviated as d in the forthcoming derivations.

Referring to Fig. 4, the average current can be obtained by dividing the total shadowed area denoted as S_1, S_2, and S_3 as

$$\begin{cases} S_1=\frac{1}{2}\left\{i_g\left[\left(k+\frac{d}{2}\right)T_s\right]+i_g[kT_s]\right\}\cdot\frac{d}{2}T_s \\ S_2=\frac{1}{2}\left\{i_g\left[\left(k+1-\frac{d}{2}\right)T_s\right]+i_g\left[\left(k+\frac{d}{2}\right)T_s\right]\right\}\cdot(1-d)T_s \\ S_3=\frac{1}{2}\left\{i_g\left[(k+1)T_s\right]+i_g\left[\left(k+1-\frac{d}{2}\right)T_s\right]\right\}\cdot\frac{d}{2}T_s. \end{cases} \tag{8}$$

Hence, the average inverter current at the kth control period can be derived as

$$\begin{aligned}\overline{i_g}[kT_s] &= \frac{S_1+S_2+S_3}{T_s} \\ &= i_g[kT_s] \\ &\quad + \frac{\{v_{\rm Cac}[k]-v_{\rm dc}[k]-v_{\rm pcc}[k]\}\,T_s+2dT_s v_{\rm dc}[k]}{2L}. \quad (9)\end{aligned}$$

Furthermore, the instantaneous current at the $(k+1)$th sampling instant can be obtained from (7) as

$$\begin{aligned}&i_g\,[(k+1)T_s] \\ &\quad = i_g[kT_s]+\frac{\{v_{\rm Cac}[k]-v_{\rm dc}[k]-v_{\rm pcc}[k]\}\,T_s+2dT_s v_{\rm dc}[k]}{L}.\end{aligned} \quad (10)$$

Therefore, from (9) and (10), the instantaneous current at the $(k+1)$th sampling instant is derived as

$$\begin{aligned}&i_g\,[(k+1)T_s] \\ &\quad = \overline{i_g}[kT_s]+\frac{\{v_{\rm Cac}[k]-v_{\rm dc}[k]-v_{\rm pcc}[k]\}\,T_s+2dT_s v_{\rm dc}[k]}{2L}.\end{aligned} \quad (11)$$

Hence, the duty cycle is rewritten in terms of the average current of the kth sampling period as

$$\begin{aligned}d[k] &= \frac{L\left\{i_g\,[(k+1)T_s]-\overline{i_g}[kT_s]\right\}}{v_{\rm dc}[k]T_s} \\ &\quad + \frac{v_{\rm dc}[k]+v_{\rm pcc}[k]-v_{\rm Cac}[k]}{2v_{\rm dc}[k]}. \quad (12)\end{aligned}$$

In (12), the term L/T_s is denoted as the current controller gain derived from the deadbeat control law. Therefore, the control signal of the VSI can be represented as

$$\begin{aligned}t_d[k] &= \underbrace{\frac{L\left\{i_g\,[(k+1)T_s]-\overline{i_g}[kT_s]\right\}}{v_{\rm dc}[k]}}_{t_d^{\rm fb}[k]} \\ &\quad + \underbrace{\frac{\{v_{\rm dc}[k]+v_{\rm pcc}[k]-v_{\rm Cac}[k]\}\,T_s}{2v_{\rm dc}[k]}}_{t_d^{\rm ff}[k]}. \quad (13)\end{aligned}$$

Equations (7) and (12) imply that the controller gain of the average current tracking scheme is twice the value of the instantaneous tracking scheme. However, the aforementioned deadbeat control scheme is based on the reduced order model of the LCL filter. Hence, the performance of the current tracking scheme might be imperfect due to a model mismatch. Therefore, the stability and robustness analysis of the current controller would be presented in the forthcoming sections.

2) AC-Side Capacitor Voltage Estimation Scheme: Referring to Fig. 1, neglecting the RC ripple filter, then the following differential equation can be derived

$$\begin{cases} v_o - v_{\rm pcc} = L\frac{di_g}{dt} - v_{\rm Cac} \\ v_{\rm Cac} = -\frac{1}{C_{\rm ac}}\int i_g dt. \end{cases} \quad (14)$$

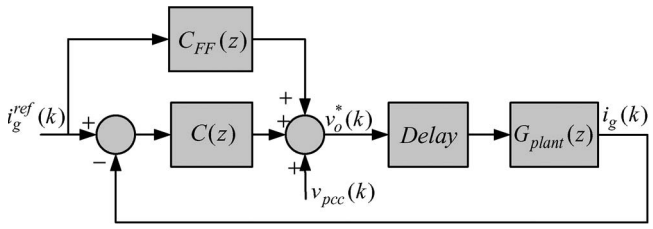

Fig. 5. Control diagram of the current loop, with ac-side capacitor voltage estimation using reference current feedforward scheme.

Discretizing (14) using the backward Euler method, we get

$$v_o^*(k)-v_{\rm pcc}(k)=L\frac{i_g(k+1)-i_g(k)}{T_s}+v_{\rm Cac}^*(k)+\frac{T_s}{C_{\rm ac}}i_g(k+1). \quad (15)$$

In order to track the reference signal and achieve deadbeat control, the current at the $(k+1)$th sampling interval $i_g(k+1)$ should be replaced by the reference signal at the next sampling cycle [6]. Hence, (15) can be written as

$$v_o^*(k)-v_{\rm pcc}(k)=L\frac{i_g^{\rm ref}(k)-i_g(k)}{T_s}+v_{\rm Cac}^*(k)+\frac{T_s}{C_{\rm ac}}i_g^{\rm ref}(k). \quad (16)$$

From (16), the current loop controller (CC) block diagram is derived as shown in Fig. 5, where $C(z)=kL/T_s$ represents the CC, $C_{\rm FF}(z)=T_s/[C_{\rm ac}(z-1)]$ represents the ac-side capacitor voltage feedforward, and $G_{\rm plant}(z)$ represents the discrete (z-domain) model of the HAPF, which is given in Appendix B.

From Fig. 5, the closed-loop transfer function is derived as

$$H_{\rm close}(z)=\frac{[C(z)+C_{\rm FF}(z)]\,G_{\rm plant}(z)G_{\rm delay}(z)}{1+C(z)G_{\rm plant}(z)G_{\rm delay}(z)} \quad (17)$$

where $G_{\rm delay}(z)$ represents the control delay. The equivalent open-loop transfer function of (17) can be obtained as

$$H_{\rm open,eq}(z)=\frac{[C(z)+C_{\rm FF}(z)]\,G_{\rm plant}(z)G_{\rm delay}(z)}{1-C_{\rm FF}(z)G_{\rm plant}(z)G_{\rm delay}(z)}. \quad (18)$$

Fig. 6 shows the open-loop Nichols plot and the closed-loop root locus of the current loop when $k=0.33$ with control delay $T_d=1.5T_s$, which accounts for the one cycle PWM control delay and a half cycle delay due to the RFs. Fig. 6(a) shows that the system is stable with a gain margin (GM) of 8.6 dB and a phase margin (PM) of 58.4°. Moreover, Fig. 6(b) shows that the dominant poles are critically damped, and a real pole is located at $p=0.98$. The left-plane conjugate poles are located at 4.21 kHz with a damping ratio of $\xi=0.18$, which results from the LCL-filer high-frequency resonance.

3) Robustness Analysis Under Model Uncertainties: Fig. 7 shows the root locus, step response, and closed-loop Bode plot of the current controller when $\Delta L_c=\pm 0.2$ p.u.. Fig. 7(a) shows that, when $\Delta L_c=-0.2$ p.u., the damping ratio of the dominant poles reduces to 0.55, the overshoot in the step response increases by 0.17 p.u., and the closed-loop bandwidth is 2.1 kHz. Fig. 7(b) shows that, in the case of $\Delta L_c=0.2$ p.u., the damping ratio of the dominant poles increases to 0.9, the overshoot in the step response increases by 0.04 p.u., and the closed-loop bandwidth is 1.4 kHz. Therefore, under a large

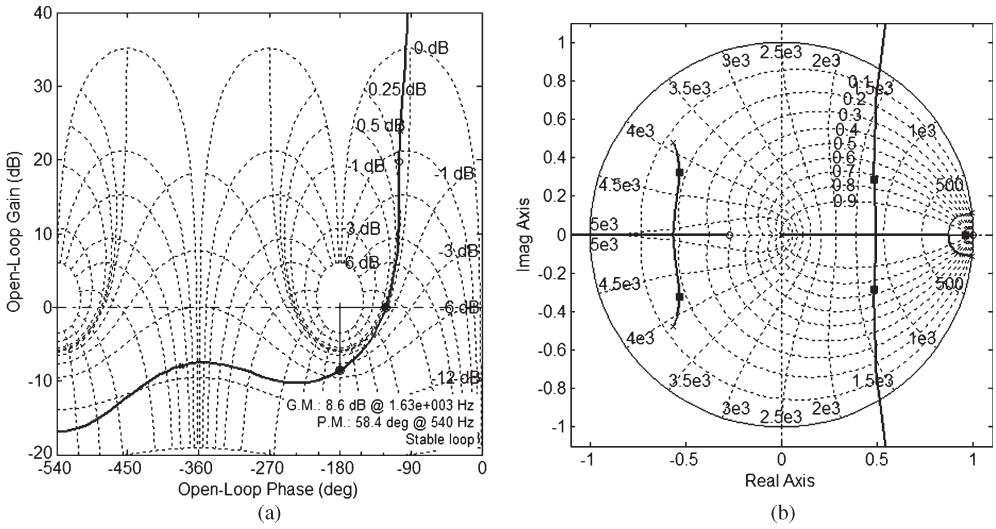

Fig. 6. Open-loop Nichols plot and closed-loop root locus when $T_d = 1.5T_s$.

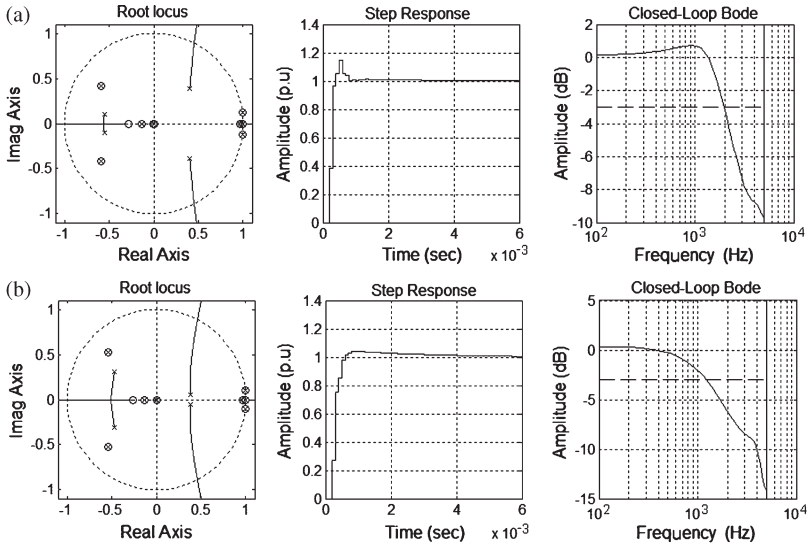

Fig. 7. Robustness of the current loop with the variation of L_c. (a) $\Delta L_c = -0.2$ p.u. (b) $\Delta L_c = 0.2$ p.u.

variation in L_c, the current loop is also stable at the tradeoff of the reduced compensation precision.

Fig. 8 shows the root locus, step response, and closed-loop Bode plot of the current controller when $\Delta C_{\rm ac} = \pm 0.2$ p.u. It is found that the parameter variation in $C_{\rm ac}$ has a negligible effect on the poles of the CC. However, the steady-state error in the current loop is proportional to the variation in $C_{\rm ac}$. Fig. 9 shows the performance evaluations of the CC with parameter variations when the step increase of the reactive current is used as a reference signal. It shows that, when $\Delta L_c = \pm 0.2$ p.u., the current tracking performance is almost the same as that in the case under nominal parameters. Nevertheless, when $\Delta C_{\rm ac} = -0.2$ and 0.2p.u., the tracking error reaches 0.1 and 0.2 p.u., respectively. However, the capacitance seldom undergoes significant variations for the practical systems.

The robustness of the current loop under the variation in L_g, C_f, and R_f is listed in Table II. It shows that the variation in L_g affects the overshoot in the step response. The variation in C_f and R_f mainly affects the position of the conjugate poles in the left half plane. Within the compensation bandwidth of the HAPF, the effect of the $\pm$0.2-p.u. variation in L_g, C_f, and R_f can be neglected.

4) AC-Side Capacitor Voltage Estimation Scheme: The HAPF-compensating current can be denoted by using the grid-side current of the LCL filter as

$$\begin{aligned} i_{\rm ga}(t) &= \sum_{n=1}^{N} I_{{\rm ga},n} \sin(n\omega_0 t + \varphi_{{\rm ga},n}) \\ &= a_{\rm ga,1} \sin(\omega_0 t + \varphi_{\rm PLL}) + b_{\rm ga,1} \cos(\omega_0 t + \varphi_{\rm PLL}) \\ &\quad + \sum_{n=3}^{N} [\cos\varphi_{{\rm ga},n} \sin(n\omega_0 t) + \sin\varphi_{{\rm ga},n} \cos(n\omega_0 t)] \\ &\quad \cdot I_{{\rm ga},n} \end{aligned} \tag{19}$$

where $a_{\rm ga,1} = I_{\rm ga,1}\cos(\varphi_{\rm ga,1} - \varphi_{\rm PLL})$ and $b_{\rm ga,1} = I_{\rm ga,1}\sin(\varphi_{\rm ga,1} - \varphi_{\rm PLL})$ represent the amplitude of the fundamental active and reactive components of the APF current and N represents the number of the highest harmonic

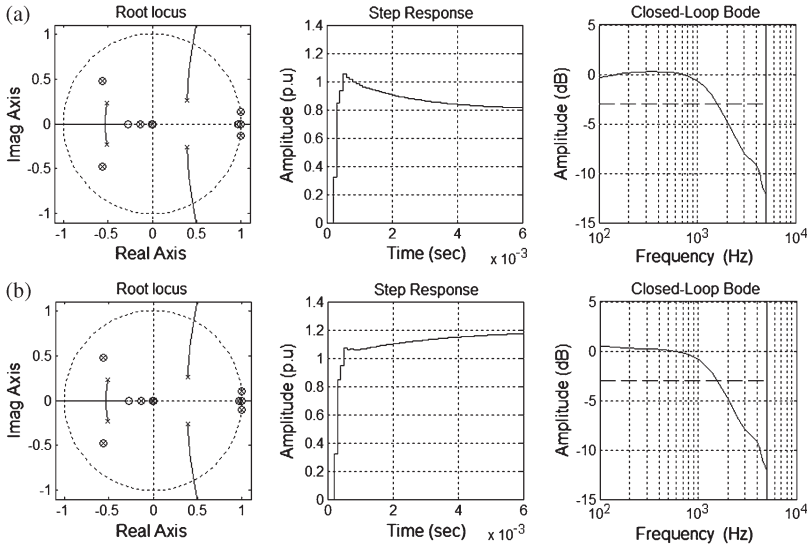

Fig. 8. Robustness of the current loop with variation of $C_{\rm ac}$. (a) $\Delta C_{\rm ac} = -0.2$ p.u. (b) $\Delta C_{\rm ac} = 0.2$ p.u.

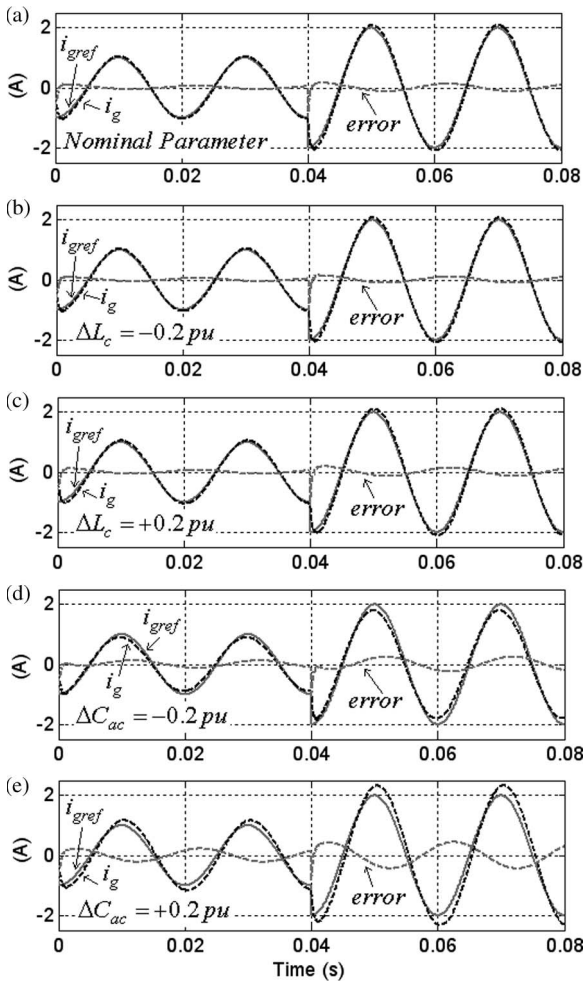

Fig. 9. Performance evaluations of the CC. (a) Under nominal parameters. (b) and (c) $\Delta L_c = -0.2$ and 0.2 p.u. (d) and (e). $\Delta C_{\rm ac} = -0.2$ and 0.2 p.u.

component compensated by the APF. Moreover, $\varphi_{\rm PLL}$ represents the initial phase angle of the PLL [29], synchronized with the fundamental component of the grid voltage. The symbols $I_{{\rm ga},n}$ and $\varphi_{{\rm ga},n}$ ($3 \le n \le N$, where n is an integer) represent the amplitude and phase of the nth-order harmonic component

TABLE II
STEP RESPONSE OVERSHOOT AND CLOSED-LOOP BANDWIDTH OF THE CURRENT LOOP WITH THE VARIATION OF L_g, C_f, AND R_f

Parameters	Overshoot	Bandwidth	Remarks
ΔL_g=-0.2pu	0.14pu	1.85kHz	Negligible effect
ΔL_g=+0.2pu	0.05pu	1.68kHz	
ΔC_f=-0.2pu	0.11pu	1.61kHz	Position of the high
ΔC_f=+0.2pu	0.07pu	1.97kHz	frequency pole
ΔR_f=-0.2pu	0.10pu	1.78kHz	Loss and damping
ΔR_f=+0.2pu	0.09pu	1.82kHz	Negligible effect

of the APF current, respectively. Notably, the noncharacteristic or even-order harmonics can be easily incorporated in the case of the half-wave rectifier loads. Supposing that the APF current is represented by $i_{\rm ga}(t)$, then the voltage drop across the ac-side capacitor $C_{\rm ac}$ is represented as

$$\begin{aligned} v_{\rm Cac}(t) &= -\sum_{n=1}^{N} I_{{\rm ga},n}\|Z_{{\rm Cac},n}\|\sin\left(n\omega_0 t + \varphi_{{\rm ga},n} - \frac{\pi}{2}\right) \\ &= a_{{\rm ga},1}\|Z_{{\rm Cac},1}\|\cos(\omega_0 t + \varphi_{\rm PLL}) \\ &\quad - b_{{\rm ga},1}\|Z_{{\rm Cac},1}\|\sin(\omega_0 t + \varphi_{\rm PLL}) \\ &\quad - \sum_{n=3}^{N}\|Z_{{\rm Cac},n}\|\cdot[I_{{\rm ga},n}\sin\varphi_{{\rm ga},n}\sin(n\omega_0 t) \\ &\quad\qquad - I_{{\rm ga},n}\cos\varphi_{{\rm ga},n}\cos(n\omega_0 t)] \end{aligned} \tag{20}$$

where $\|Z_{{\rm Cac},n}\|$ (n is an integer) represents the nth-order harmonic impedance of the capacitor $C_{\rm ac}$. Notably, the phase angle of the ac-side capacitor $v_{\rm Cac}(t)$ is lagging the APF current $i_{\rm ga}(t)$ by 90°.

Therefore, the feedforward voltage in the current controller can be derived as

$$\begin{aligned} i_{\rm ga,ff}^{\rm ref}(t) &= i_{\rm La}(t) - I_{\rm La,1}\cos(\varphi_{\rm La,1} - \varphi_{\rm PLL}) \\ &\quad \times \sin(\omega_0 t + \varphi_{\rm PLL}) \\ &= b_{\rm La,1}\cos(\omega_0 t + \varphi_{\rm PLL}) \\ &\quad + \sum_{n=3}^{N}[a_{{\rm La},n}\sin(n\omega_0 t) + b_{{\rm La},n}\cos(n\omega_0 t)]\,. \end{aligned} \tag{21}$$

Under this scenario, i.e., the nonactive component of the load-side current is utilized as the feedforward current, then the virtual voltage drop across the ac-side capacitor $C_{\rm ac}$ can be represented by

$$\begin{aligned} v_{\rm Cac,ff}^{\rm ref}(t) =& -\sum_{n=1}^{N} I_{{\rm La},n}\sin\left(n\omega_0 t+\varphi_{{\rm La},n}-\frac{\pi}{2}\right)\|Z_{{\rm Cac},n}\| \\ &+ I_{\rm La,1}\cos(\varphi_{\rm La,1}-\varphi_{\rm PLL}) \\ &\times \sin\left(\omega_0 t+\varphi_{\rm PLL}-\frac{\pi}{2}\right)\|Z_{\rm Cac,1}\| \\ =& -b_{\rm La,1}\|Z_{\rm Cac,1}\|\sin(\omega_0 t+\varphi_{\rm PLL}) \\ &-\sum_{n=3}^{N}\|Z_{{\rm Cac},n}\| \\ &\cdot\left[b_{{\rm La},n}\sin(n\omega_0 t)-a_{{\rm La},n}\cos(n\omega_0 t)\right] \end{aligned} \tag{22}$$

where $a_{{\rm La},n}$ and $b_{{\rm La},n}$ ($3\le n\le N$, where n is an integer) represent the weights of the harmonic component obtained from the ADALINE identifier (see Fig. 2). Furthermore, the active current of the VSI $\Delta I_p\sin(\omega_0 t+\varphi_{\rm PLL})$, generated by the dc-voltage loop, would also have a voltage drop across the capacitor $C_{\rm ac}$, which is denoted as

$$\begin{aligned} v_{\Delta I_p} =& \Delta I_p\|Z_{\rm Cac,1}\|\sin\left(\omega_0 t+\varphi_{\rm PLL}-\frac{\pi}{2}\right) \\ =& -\Delta I_p\|Z_{\rm Cac,1}\|\cos(\omega_0 t+\varphi_{\rm PLL}). \end{aligned} \tag{23}$$

From (22) and (23), the voltage drop across the capacitor $C_{\rm ac}$ in the feedforward loop is derived as

$$\begin{aligned} v_{\rm Cac,ff}^{\rm ref}(t) =& -\left(b_{\rm La,1}\sin(\omega_0 t+\varphi_{\rm PLL})\right. \\ &\left.+\Delta I_p\cos(\omega_0 t+\varphi_{\rm PLL})\right)\|Z_{\rm Cac,1}\| \\ &-\sum_{n=3}^{N}\|Z_{{\rm Cac},n}\| \\ &\cdot\left[b_{{\rm La},n}\sin(n\omega_0 t)-a_{{\rm La},n}\cos(n\omega_0 t)\right]. \end{aligned} \tag{24}$$

Hence, the feedforward control signal is obtained as

$$t_d^{\rm ff}[k]=\frac{\left\{v_{\rm dc}[k]+v_{\rm pcc}[k]-v_{\rm Cac,ff}^{ref}[k]\right\}T_s}{2v_{\rm dc}[k]}. \tag{25}$$

Therefore, (25) can be substituted into (13) to synthesize the total modulation signal.

5) Stability Analysis of the Grid Current Feedback Loop: To enhance the compensation precision of the HAPF, the grid current feedback loop is also incorporated in the current controller (see Fig. 2). The synchronous reference frame (SRF) detection method is used to extract the individual harmonic component from the grid current (see Fig. 10). The grid current is multiplied by $\sin(n\omega_n t+\theta_n)$ and $\cos(n\omega_n t+\theta_n)$, followed by low-pass filters (LPFs) to extract the dc component, and then multiplied by the *sine* and *cosine* functions to reconstruct the nth harmonic component. The delay compensation for the RF is achieved by adding the leading phase φ_n to the phase angle.

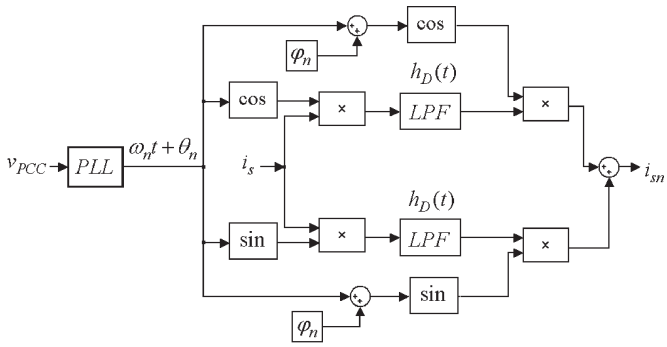

Fig. 10. Individual harmonic extraction algorithm for grid current feedback loop based on the SRF detection method.

Referring to Fig. 10, the transfer function for the feedback estimation scheme can be derived as [31]

$$G_{\rm fb}(s)=\sum_{n\in N_h}\frac{k_n\cos(\varphi_n)\cdot\left[s+\frac{1}{\tau_n}-\omega_n\frac{\sin(\varphi_n)}{\cos(\varphi_n)}\right]}{s^2+\frac{2}{\tau_n}s+\left(\omega_n^2+\frac{1}{\tau_n^2}\right)} \tag{26}$$

where τ_n is the time constant of the LPF and k_n represents the feedback gain for the nth harmonic component. The selection of the cutoff frequency of the LPF (normally less than 5 Hz) and k_n is a tradeoff between the harmonic rejection capability and the closed-loop stability [31].

Fig. 11 shows the open-loop Bode plot and closed-loop root locus of the grid current feedback loop, where $\tau_n=0.63$ and $k_n=\{330,260,170,150,130,80\}$ for the 3rd- to the 13th-order harmonics. Fig. 11(a) shows that the GM is 8.53 dB and PM is 11.6°. Fig. 11(b) shows that the closed-loop poles are within the unit circle. These poles can be moved into the circle by reducing the feedback gain at the cost of reducing the open loop gain of the grid current feedback loop.

D. DC-Link Voltage Control

In order to ensure stable operation of the APF, the difference between the dc-link voltage and its reference is regulated by using a proportional–integral (PI) controller, and the output of the PI regulator is multiplied by a unit *sine* signal generated by the PLL to synthesize the reference for the active current for the current loop (see Fig. 2). The guidelines for the dc-link voltage setting of APFs have been presented in [32]. In this paper, the dc-link reference of 300 V is chosen to reach a compromise among the dc-link ripple, switching loss, EMI injection, and the size and cost of the output LCL filter.

IV. Experimental Results

To verify the validity of the devised control algorithms, a 75-kVA prototype system was built, using three single-phase VSI topologies (see Fig. 12). Fig. 13 shows the architecture of the main controller. The three single-phase VSIs are controlled independently based on using the dual digital signal processor (DSP) plus field-programmable gate array (FPGA) controller platforms. The voltage and current signals are sampled using two analog/digital (A/D) chips (ADS8364) after being preprocessed by the RFs, where the input analog signals are

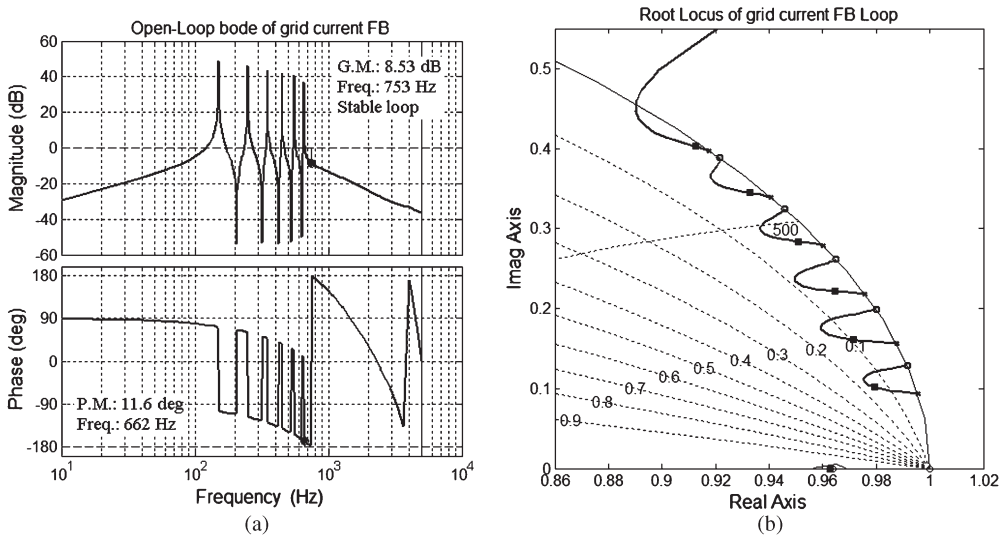

Fig. 11. Open-loop Bode diagram and the closed-loop root locus of the grid current feedback loop.

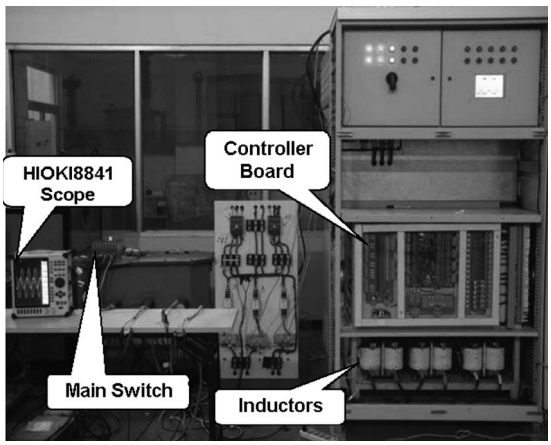

Fig. 12. Photograph of the prototype system using three single-phase topologies.

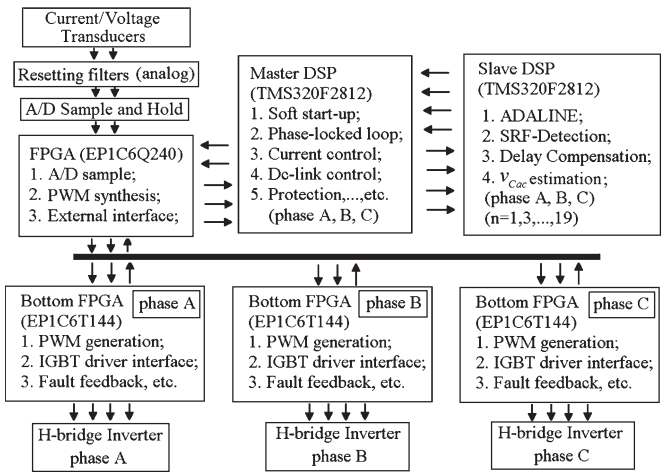

Fig. 13. Architecture of the main controller platform.

filtered by analog integration circuits. The resetting signals are generated by the FPGA in the main controller, using the 10-kHz pulses. The sampled data are buffered in the FPGA, which are read by the timer interrupt of the master DSP.

The master DSP is responsible for the soft startup, software PLL, current control, and dc-link control as well as the overvoltage and overcurrent protection. The slave DSP is used for the ac-side capacitor voltage estimation and the SRF-based reference generation algorithm. The master and slave DSPs achieve parallel data transfer by using a dedicated FPGA, which serves as the dual port random access memory. Three ADALINE structures are implemented for load current estimation, and the delay compensation due to sampling and master/slave-DSP communication is achieved by adding the leading phase angle for the individual harmonics. The PWM signals are generated by the master DSP and sent to the FPGA in the main controller board. These signals are sent to the bottom controller board in each inverter. Additionally, the gating signals are processed by the bottom FPGA to synthesize four PWM signals after a dead time of 4 μs is added.

Fig. 14 shows the experimental results of three single-phase thyristor rectifiers with a resistive load of 2.2 Ω when the firing angle $= 100^{\circ}$. Before the APF is switched on, an obvious notch can be observed in the grid voltage at the conduction instant of the thyristor load due to the remarkable grid impedance [see Fig. 14(a)]. The load currents are highly distorted with significant di/dt at the rising and falling edges, with a total harmonic distortion (THD) of 76%, characterized by the odd harmonics, which is the typical scenario for the harmonic contamination for the residential and industrial customers.

Fig. 14(b) shows the experimental results when the HAPF starts the compensation. Notably, a fixed compensation of 30-A reactive current is generated by the APF. The harmonics of the odd order up to the 19th order are selected in the feedforward and feedback loops. It can be observed that excellent sinusoidal waveforms are achieved at the source side, with a THD of less than 6.5%. Moreover, the neural wire current is also minimized.

Fig. 15 shows the experimental results of the HAPF for the unbalanced nonlinear load, which is composed of the three single-phase thyristor loads and a single-phase diode rectifier

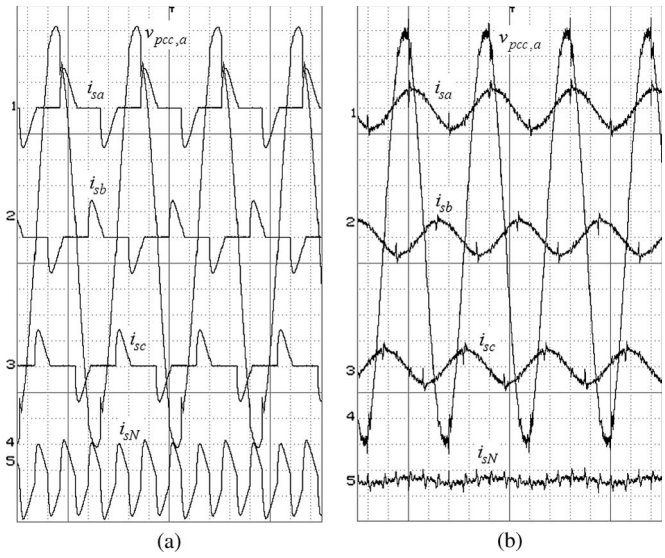

Fig. 14. Experimental results for the three single-phase thyristor rectifier. The results (a) before compensation and (b) after compensation ($v_{\mathrm{pcc,a}}$: 20 V/div; i_{sa}, i_{sb}, i_{sc}, i_{sN}: 80 A/div; x-axis: 5 ms/div).

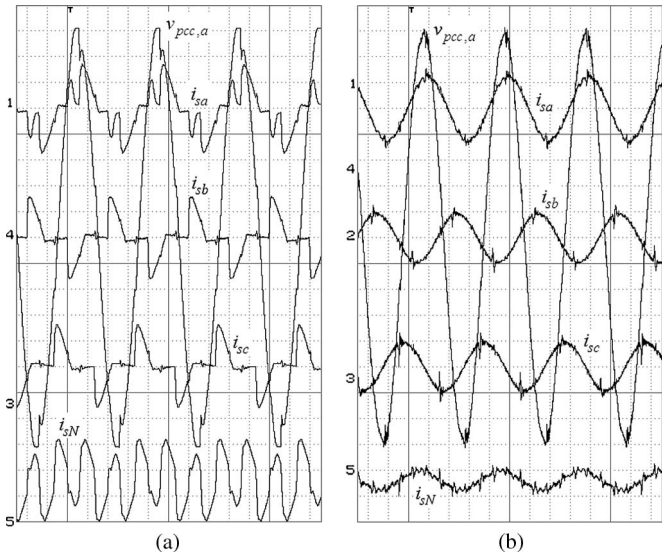

Fig. 15. Experimental results for the unbalanced three-phase load. The results (a) before compensation and (b) after compensation ($v_{\mathrm{pcc,a}}$: 20 V/div; i_{sa}, i_{sb}, i_{sc}, i_{sN}: 80 A/div; x-axis: 5 ms/div).

connected between phase "a" and the neutral wire. The circuit parameters of the thyristor rectifier load are the same as those adopted in the previous case. The dc side of the single-phase diode rectifier consists of a 15-Ω resistor shunt connected with a capacitor of 5000 μF. Fig. 15(a) shows that the source-side current is highly distorted in phase "a," with a THD of 85%, and the currents in phase "b" and "c" are almost same as those in Fig. 14(a). Fig. 15(b) shows the results when the HAPF is in operation with a fixed reactive current injection of 30 A. It can be observed that the source-side currents are sinusoidal with a THD of 5%, and the neutral current is also harmonic free.

Fig. 16(a) shows the experimental results when the HAPF is suddenly switched on. The dc-link capacitor is precharged to limit the APF currents during transients. Fig. 16(b) shows the results when the HAPF generates a constant reactive current of

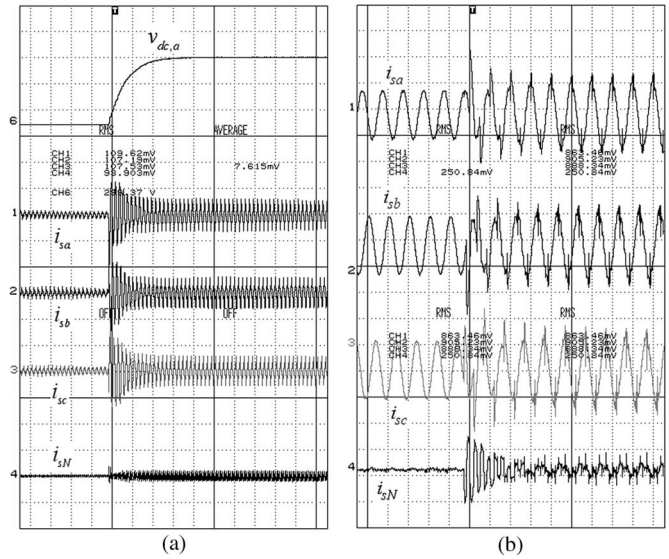

Fig. 16. Transient response of the HAPF. (a) Sudden turn-on of the HAPF ($v_{\mathrm{dc,a}}$: 20 V/div; i_{sa}, i_{sb}, i_{sc}, i_{sN}: 80 A/div; x-axis: 100 ms/div). (b) Load is suddenly switched on (i_{sa}, i_{sb}, i_{sc}, i_{sN}: 80 A/div; x-axis: 20 ms/div).

30 A and a sudden turn-on of the three single-phase thyristor rectifier loads (firing angle $= 90^{\circ}$) is applied. It shows that the grid current tracks the sudden increase of load within one cycle.

Figs. 14–16 imply that the proposed HAPF is very effective for compensating the nonlinear load current with sharp rising and falling edges, and the devised ADALINE scheme is proven to be a perfect real-time harmonic estimation method, which can be easily inserted in the existing algorithms by adding subroutines for the reference current.

V. Conclusion

This paper has proposed a novel LCL-filter-based HAPF topology, using the single-phase hybrid LCL-filter structures. The proposed HAPF shows the advantage of the conventional HAPF due to the reduced dc-link voltage compared to the pure APF based on the L filter or LCL filter as the interfacing impedance. Moreover, the LCL-filter section provides perfect high-frequency characteristics with significant reduction of the switching ripples and the EMI injection to the electric distribution system.

The mathematical model of the HAPF is derived by using state-space representations. The RFs are adopted as the preprocessing units for the sampling signals to enhance the controller robustness. The feedforward plus feedback control scheme is used to achieve excellent steady-state precision and dynamic performance. To alleviate the CC design, the ac-side capacitor voltage is estimated using the ADALINE identifier from the load current. The grid current feedback using the SRF detection scheme is used to enhance the compensation precision of the HAPF.

A 75-kVA laboratory prototype system is built for verification. The dual DSPs and FPGA are used as the main controller to implement the devised algorithms. The effectiveness of the proposed HAPF and its control algorithms are validated by the experimental results.

APPENDIX A

$$\mathbf{A_{c0}} = \begin{bmatrix} -\frac{R_{f0}}{L_{g0}} & \frac{R_{f0}}{L_{g0}} & \frac{1}{L_{g0}} & \frac{1}{L_{g0}} \\ \frac{R_{f0}}{L_{c0}} & -\frac{R_{f0}}{L_{c0}} & 0 & -\frac{1}{L_{c0}} \\ -\frac{1}{C_{\mathrm{ac}0}} & 0 & 0 & 0 \\ -\frac{1}{C_{f0}} & \frac{1}{C_{f0}} & 0 & 0 \end{bmatrix}$$

$$\mathbf{B_{c0}} = \mathrm{diag}(0, 1/L_{c0}, 0, 0)$$

$$\mathbf{G_{c0}} = \mathrm{diag}\left(\frac{1}{L_{g0}}, \frac{1}{L_{c0}}, \frac{1}{C_{\mathrm{ac}0}}, \frac{1}{C_{f0}}\right)$$

$$\mathbf{C} = \mathrm{diag}(1, 0, 0, 0).$$

APPENDIX B

The s-domain model of the HAPF power stage is derived as

$$G_{\mathrm{plant}}(s) = \frac{I_g(s)}{V_0(s)} = \frac{a_2 s^2 + a_1 s}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad \text{(B.1)}$$

where the parameters $a_2 = R_f$, $a_1 = 1/C_f$, $b_4 = L_g L_c$, $b_3 = (L_g + L_c)R_f$, $b_2 = (L_g + L_c)/C_f + L_c/C_{\mathrm{ac}}$, $b_1 = R_f/C_{\mathrm{ac}}$, and $b_0 = 1/(C_f C_{\mathrm{ac}})$. The z-domain model can be derived using the zero-order hold (ZOH) as

$$G_{\mathrm{plant}}(z) = Z\left\{\underbrace{\frac{1 - e^{-sT_s}}{s}}_{H_{\mathrm{zoh}}(s)} G_{\mathrm{plant}}(s)\right\} = \frac{z-1}{z} Z\left\{\frac{G_{\mathrm{plant}}(s)}{s}\right\}. \quad \text{(B.2)}$$

Substituting the nominal parameters into (B.2), we get

$$G_{\mathrm{plant}}(z) = \frac{0.1066z^3 + 0.09528z^2 - 0.1553z - 0.0466}{z^4 - 0.8584z^3 - 0.693z^2 + 0.03803z + 0.5488}. \quad \text{(B.3)}$$

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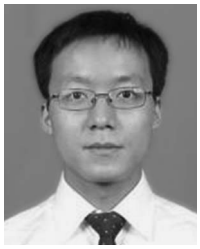

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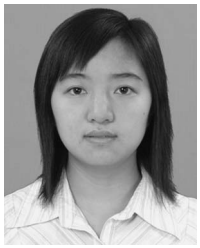

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