# Variable Interleaving Technique for Photovoltaic Cascaded DC-DC Converters

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***Abstract*—This paper introduces a variable interleaving technique for photovoltaic cascaded DC-DC converters. A series rather than parallel connection of converters allows higher switch utilization and lower rating of components; however, they suffer from nonhomogeneous irradiations condition. Under partial shading conditions, the input power of all PV panel will not be the same and as a result the output voltage of each converter will not be identical. This causes system to operate in an asymmetric condition, in which, the conventional interleaving techniques are not capable of eliminating the DC link output voltage variations. In this work, an interleaving algorithm is reported on cascaded DC/DC converters under asymmetric condition to minimize the DC link output voltage variations. The effectiveness of this algorithm for cascaded DC-DC converters has been validated by simulation and Hardware-In-the-Loop tests.**

***Keywords— photovoltaic (PV), Maximum power point tracking (MPPT), Incremental conductance (IncCond,) Variable Interleaving (VI),***

## I. INTRODUCTION

The global electrical energy consumption is rising and there is a steady increase in the demand for higher power capacity, efficient production, distribution and utilization of energy. Photovoltaic (PV) power supplied to the utility grid, as a renewable energy, is gaining more and more visibility, while the world's power demand is increasing [1].

The power electronic technology has an essential role to match the characteristics of the PV generation units and the demand of the grid connections, including frequency, voltage, control of active and reactive power, harmonic minimization etc.; therefore, focus has been placed on new, cheap, and innovative converter solutions [2]. The cost of the grid-connected converters is gaining more and more visibility and design of a cost-effective converter with a high efficiency has become of greater interest. In this regards, many research works have been done on different kind of topologies among the parallel and series configurations for PV systems.

It has been revealed that there is a tradeoff between the cost and reliability for parallel and series converters. In parallel DC/DC converters configurations, in which each of them has its own MPPT, the reliability is higher than series connection. In the case of, e.g. partial shading on some panels or when a PV module is taken out (in case of damage or maintenance), the system is capable of working properly and the other converters will be able to follow their own MPPT to deliver the maximum power to the system. However; the parallel connected converters require high voltage fast recovery diodes and MOSFETs, which are at a performance versus cost disadvantage. On the other hand, the cascaded connection of DC/DC converters allows the input-output voltage to be close to unity which leads to low voltage switches, diodes, inductors and capacitors. Efficiencies are close to 100% and converters can be small, light and low cost [3], [4]. However; under inhomogeneous irradiation, the power generated by each PV module and the output DC voltage becomes unbalanced [5].

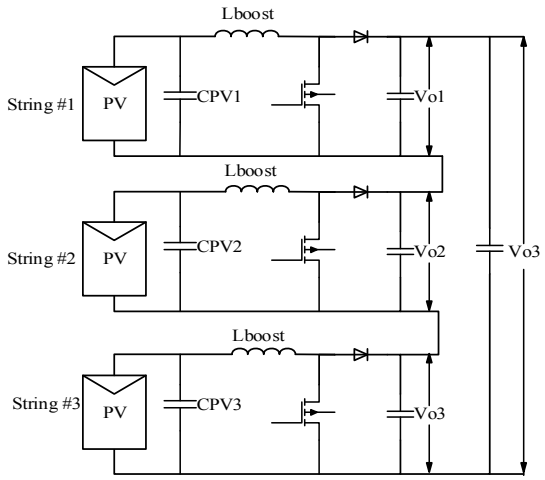



Fig.1. PV String boost converter

Unlike the parallel module integrated converters MICs, the interleaving techniques have not been studied well in series MICs.

Fig.1 shows a prototype three PV string boost converter. The DC link voltage is the sum of the individual MICs, where the string voltage ripple can be reduced by properly interleaving between each MIC. As it is depicted in Fig. 2, the standard fixed 120• interleaving algorithm significantly reduces the DC link voltage ripple in comparison to the non-interleaved system. However; this traditional interleaving

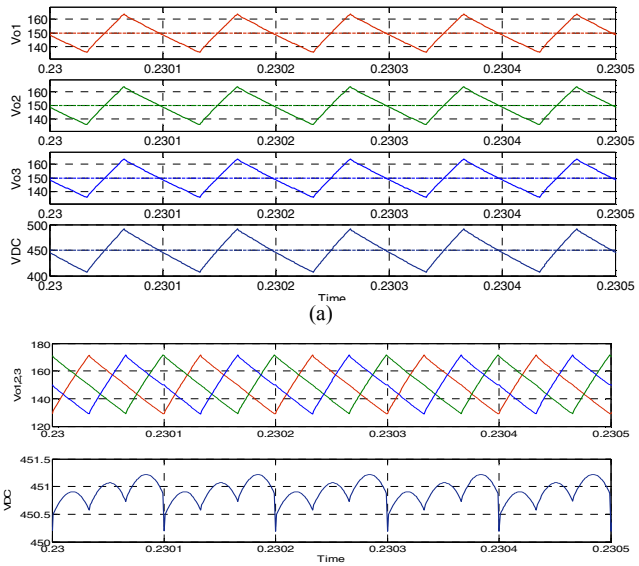



Fig.1. PV MIC output Voltages and DC link Voltage in (a) non-interleaved system and (b) Fixed-Interleaved system

technique is suitable for three exactly identical systems, which is not always true for the PV string converters. Under partial shading conditions, the input power of all PV panel will not be the same and as a result the output voltage of each converter will not be identical. The PV power varies directly with the ambient conditions and the irradiance level [6], therefore, the outputs of the PV strings can differ from each other, which causes the output voltages to become unbalanced and the system then operates under asymmetric condition.

The problem is to further minimize the DC link voltage ripple and consequently reduce the required DC link capacitance in cascaded systems especially under an asymmetric condition. The same issue for parallel connections was first addressed in [8] and a new variable interleaving algorithm was introduced. This algorithm is employed here and extended to the cascaded DC/DC converters for PV applications under asymmetric conditions.

This paper is organized as follows. In Section II, the variable interleaving algorithm in cascaded DC-DC converters is explained and the mathematical analysis is given to theoretically prove this technique. The system description and the simulation results are presented in Section III. The experimental results are demonstrated in Section IV. Section V presents the conclusions.

## II. Variable Interleaving Algorithm In Cascaded DC–DC Converter PV Architecture

### A. Structure, Operation, and Steady-State Analysis

In a series topology of per-panel DC-DC converters, a high-voltage string connected to a single DC-AC inverter or a DC load results in the input-output voltage to be close to unity which leads to low voltage switches, diodes, inductors and capacitors, and obviously cheaper but also more efficient topology than parallel connections. The buck and boost converters are the

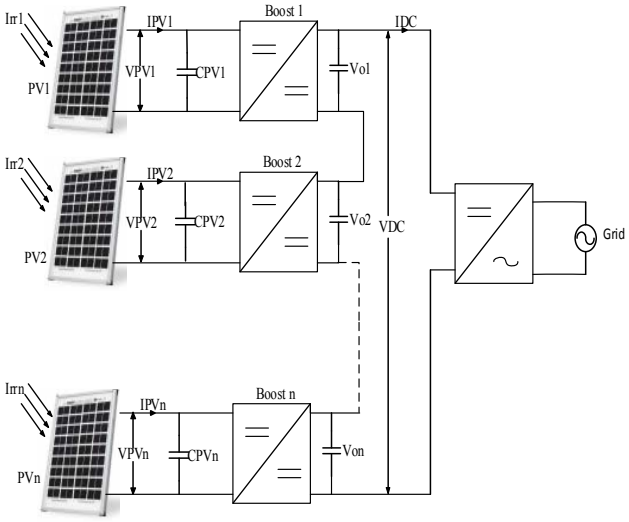



Fig.3. Block diagram of the n cascaded MIC PV architecture.

most efficient topologies for a given cost, as shown in [3]. Here, boost DC-DC converters have been employed.

The PV power alters directly with the ambient conditions and the irradiance level, therefore, the outputs of the PV strings can differ from each other. Fig.3 shows the block diagram of the n cascaded MIC. At steady state, the same current $I_{DC}$ passes through all the DC choppers, with the sum of their output voltages being the DC bus voltage (Fig.3). Let $V_{PVi}$ and $I_{PVi}$ ($i=1,2,3,..,n$), be the $n$ operating points, thus the output voltages are:

$$\sum_{i=1}^{n} V_{oi} = V_{DC} \quad (1)$$

$$P_{DC} = V_{DC}.I_{DC} = \sum_{i=1}^{n} V_{oi}.I_{DC} = \sum_{i=1}^{n} V_{PVi}.I_{PVi} \quad (2)$$

$$V_{oi} = \frac{P_{DCi}}{I_{DC}} = V_{DC}.\frac{I_{PVi}.V_{PVi}}{\sum_{i=1}^{n} I_{PVi}.V_{PVi}} \quad (3)$$

$$V_{oi} = V_{DC}.w_i \quad \text{where } i = 1,2,3,\ldots \quad (4)$$

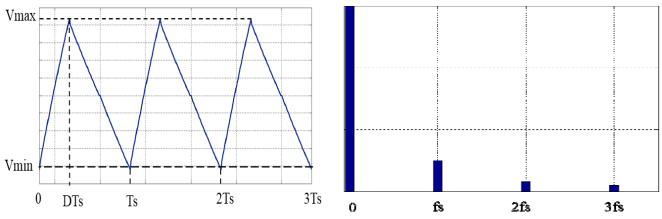
Thus, the DC-bus voltage distribution on the converter modules depends on the weights of the individual PV powers in the global power provided $w_i$. Hence, under partial shading the system will be asymmetric.

### B. Variable Interleaving Algorithm

Fig. 4 depicts the output voltage waveform of the boost converter and its spectrum. The DC link voltage is the sum of the individual MICs:

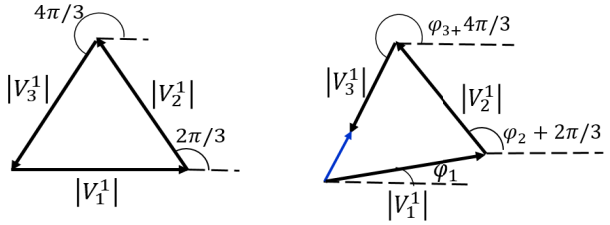
$$V_{DC} = V_{o1} + V_{o2} + V_{o3} \quad (5)$$

The fundamental frequency component equals the switching frequency. Since the first harmonic has the highest amplitude and lowest frequency, it has most impact on the DC link voltage ripple and should be minimized. Under symmetric condition, in which the weights of the individual PV powers are equal, the first harmonic component in the DC link voltage can be completely eliminated in fixed phase interleaving as




(a) (b)

Fig.4. Boost converter (a) DC output voltage and (b)its spectrum




(a) (b)

Fig.5. DC Link Voltage First harmonic component under (a) symmetric and (b) asymmetric condition

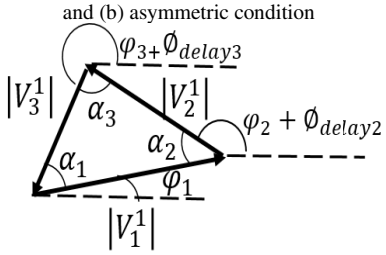



Fig.6. DC Link Voltage First harmonic component with VI method

shown in Fig.5-a. This means that the phase voltages are identical but phase shifted by 120•. Therefore, a smaller dc voltage ripple in the DC link output voltage can be obtained. However; under asymmetric condition, e.g. partial shading on some panels, the first harmonic frequency component remains in the DC link when fixed interleaving is applied (Fig. 5-b).

If the interleaving angles of the first harmonic components of each MIC voltage are properly configured, the first harmonic component in the spectrum of the DC link voltage can be completely eliminated. Fig.6 shows how the sum of them can be zero, if they form a triangle. In order to obtain the proper angles, first we need to analyze the waves in Frequency domain.

The Fourier series of a periodic waveform is expressed as:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(a_n.\cos(nwt) + b_n.\sin(nwt)) \quad (6)$$

$$a_n = \frac{2}{T}\int_0^T f(t).\cos(nwt)\,dt \quad (7)$$

$$b_n = \frac{2}{T}\int_0^T f(t).\sin(nwt)\,dt \quad (8)$$

The amplitude and phase of the first harmonic component can be obtained as follow:

$$|V_{oi}^1| = \sqrt{a_1^2 + b_1^2} \quad (9)$$

$$\varphi_i^1 = \begin{cases} \tan^{-1}\frac{b_1}{a_1} & for\ a_1 > 0 \\ \tan^{-1}\frac{b_1}{a_1} + \pi & for\ a_1 < 0 \end{cases} \quad (10)$$

According to Fig.4, the output voltage of each MIC ($V_{oi}$) in a boost DC/DC converter can be defined as [9]:

$$v_{oi} = \begin{cases} \frac{\Delta V}{DT_s}t + V_{min} & for\ 0 < t < DT_s \\ -\frac{\Delta V}{D'T_s}(t - T_s) + V_{min} & for\ DT_s < t < T_s \end{cases} \quad (11)$$

Where $T_s$ is the switching period and D is the steady state duty cycle. By using equations (7) and (8) the $a_1$ and $b_1$ can be obtained:

$$a_1 = \frac{2}{T}[\int_0^{DT_s}\left(\frac{\Delta V}{DT_s}t + V_{min}\right).cos\,(n\omega t)dt + \int_{DT_s}^{T_s}\left(-\frac{\Delta V}{D'T_s}(t - T_s) + V_{min}\right).\cos(n\omega t)\,dt] \quad (12)$$

$$b_1 = \frac{2}{T}[\int_0^{DT_s}\left(\frac{\Delta V}{DT_s}t + V_{min}\right).\sin(n\omega t)\,dt + \int_{DT_s}^{T_s}\left(-\frac{\Delta V}{D'T_s}(t - T_s) + V_{min}\right).\sin(n\omega t)\,dt] \quad (13)$$

$$a_1 = \frac{\Delta V}{2\pi^2 DD'}(cos(2\pi D) - 1) \quad (14)$$

$$b_1 = \frac{\Delta V}{2\pi^2 DD'}\sin(2\pi D) \quad (15)$$

Thus the first harmonic component of each MIC output voltage can be calculated as follow:

$$V_1^1 = |V_{01}^1|.e^{j\varphi_1^1} \quad (16)$$

$$V_2^1 = |V_{02}^1|.e^{j\varphi_2^1} \quad (17)$$

$$V_3^1 = |V_{03}^1|.e^{j\varphi_3^1} \quad (18)$$

In case of asymmetry, the phase of these components should be configured such that the sum of them becomes zero, therefore; the angles can be calculated such that they form a triangle:

$$\alpha_1 = \cos^{-1}\frac{|V_1^1|^2 + |V_3^1|^2 - |V_2^1|^2}{2|V_1^1||V_3^1|} \quad (19)$$

$$\alpha_2 = \cos^{-1}\frac{|V_1^1|^2 + |V_2^1|^2 - |V_3^1|^2}{2|V_1^1||V_2^1|} \quad (20)$$

$$\alpha_1 + \alpha_2 + \alpha_3 = 180° \quad (21)$$

Thus, the new angles of the components are:

$$\varphi_{new1}^1 = \varphi_1^1 \quad (22)$$

$$\varphi_{new2}^1 = \pi + \varphi_1^1 - \alpha_2 \quad (23)$$

$$\varphi_{new3}^1 = \pi + \varphi_1^1 + \alpha_1 \quad (24)$$

Hence, the phase delay of the PWM signals will be:

$$\emptyset_{delay1} = 0 \quad (25)$$

$$\emptyset_{delay2} = \pi + \varphi_1^1 - \varphi_2^1 - \alpha_2 \quad (26)$$

$$\emptyset_{delay3} = \pi + \varphi_1^1 - \varphi_3^1 + \alpha_1 \quad (27)$$

Note that if $V_1^1$, $V_2^1$, and $V_3^1$cannot form a triangle, two vectors with smaller amplitudes should be controlled in the same direction and the third one in the opposite direction.

TABLE I. SYSTEM DESCRIPTION

| PV Parameters | | | Boost DC/DC Converter Parameters | | |
|---|---|---|---|---|---|
| *Voc(V)* | *Isc(A)* | *MPPT V* | *Inductor (L)* | *Capacitor (C)* | *DC Bus Voltage* |
| 37.6 | 8.63 | 30.5 | 0.3 mH | 30μF | 180V |

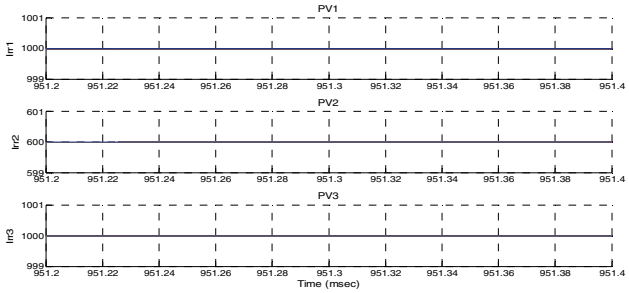



Fig.7. PV String #1,2,3 Irradiance Level

Above derivations are not complex calculations and can be simply implemented and there is no need of using online FFT.

## III. SIMULATION VERIFICATION

This section presents the simulation results of the classical three cascade topology of DC-DC MICs in order to validate the performance of the Variable Interleaving Algorithm and compare it with the traditional fixed interleaving method. Some simulations have been carried out in PSCAD [10], [11]. In these simulations, three PV modules ISOFOTON-ISF245 were used. Each PV module considered in this paper is made up of 60 PV cells connected in series providing an open circuit voltage ($V_{oc}$)=37.6V and a short circuit current ($I_{sc}$ )=8.63 A [12], [13].

Each PV generator is independently set in MPPT by the IncCond algorithm, under strongly and rapidly variable irradiance conditions [14]. The boost converters use PI-regulators for the voltage control. The parameters of the system are listed in Table I and the switching frequency is 50kHz.

All the PV generators initially operating at MPPT, under equal irradiance levels, i.e., $Irr1 = Irr2 = Irr3 = 1000$ W/m². As an example the Irr2 decreases to 600W/m$^2$ (Fig.7).

$$w_i = {I_{rri}}/{(I_{rr1} + I_{rr2} + I_{rr3})} \quad (28)$$

According to above equation the Vo2 is decreased to:

$V_{o2} = \frac{600}{2600} \times 180 = 42\,v$ and Vo1 and Vo3 are increased, which leads to the system operating in an asymmetric mode.

Fig.8 shows the output voltages for each MIC and the DC Link output voltage, when no interleaving technique is applied. As it can be seen the ripple of the DC link voltage is very high.

Fig.9 illustrates the output voltages when the fixed interleaving ($\emptyset_{delay2} = \frac{4\pi}{3} and\ \emptyset_{delay2} = 2\pi/3$) is utilized. The DC link ripple voltage in this mode is reduced in comparison with the pervious condition; however, it is not

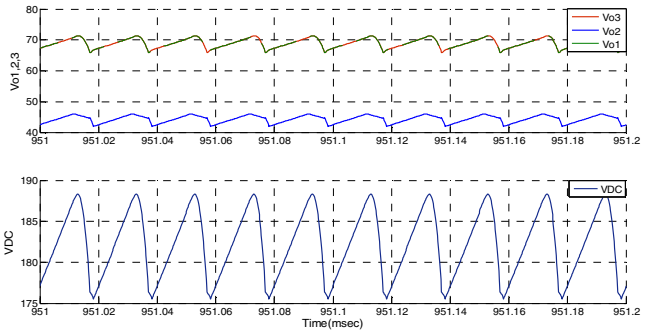



Fig.8. Output Voltages in no interleaved system

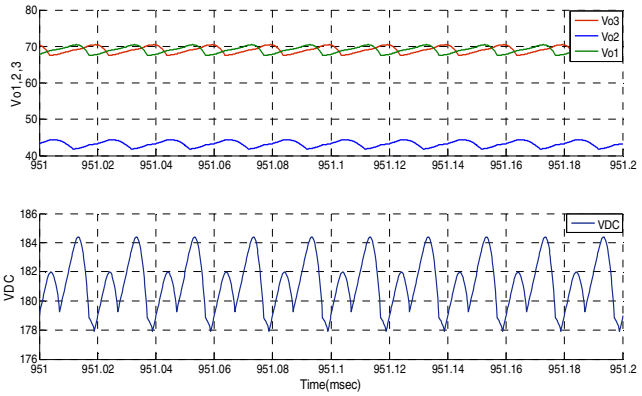



Fig.9. Output Voltages with Fixed interleaved algorithm

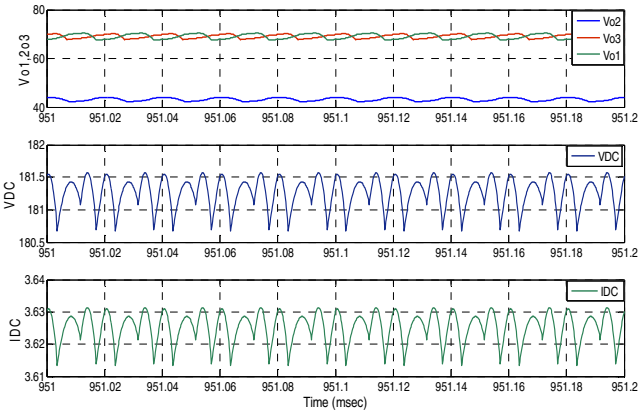



Fig.10. Output Voltages and DC current with variable interleaving algorithm

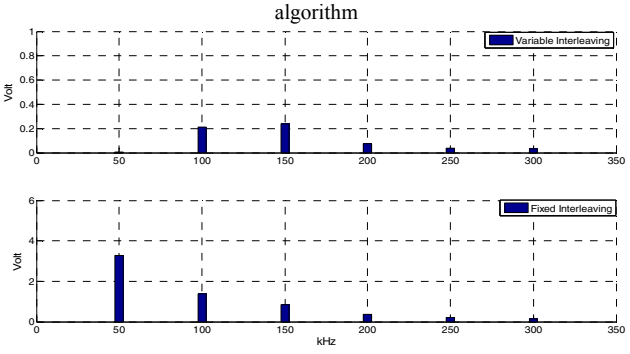



Fig.11. DC Link Voltage FFT with variable and fixed algorithm

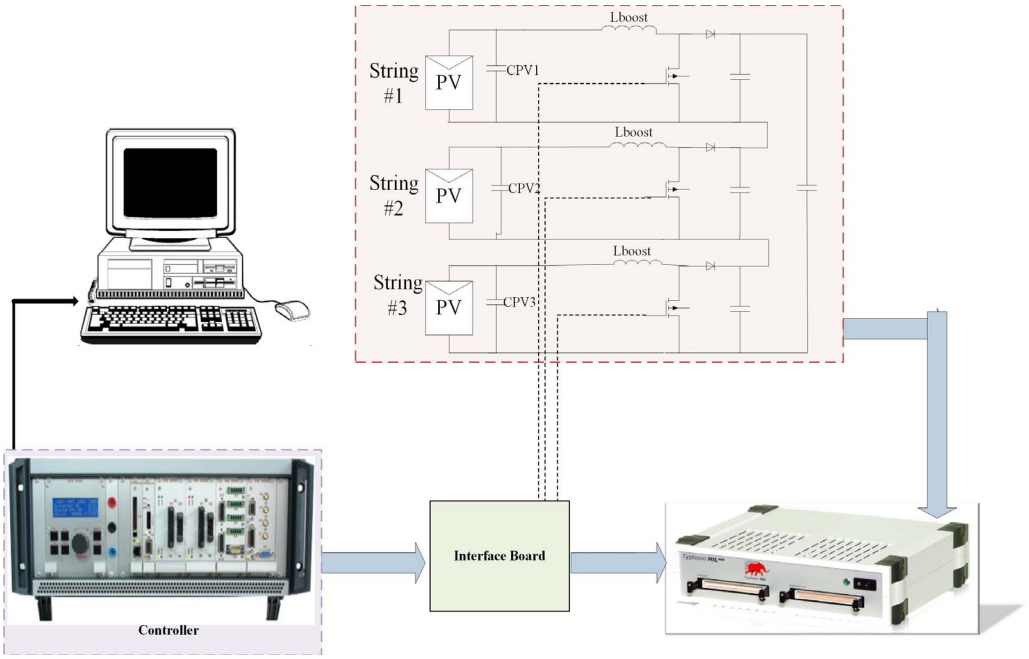



Fig.12. Hardware-in-the-Loop test system with Typhoon HIL system and AIX DSP and FPGA based controller

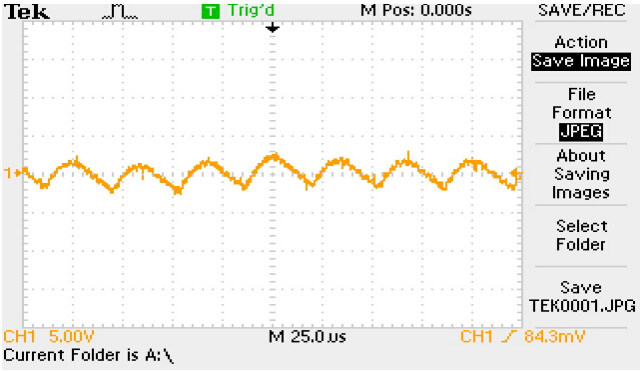



Fig.13. Output dc voltage with fixed interleaved algorithm

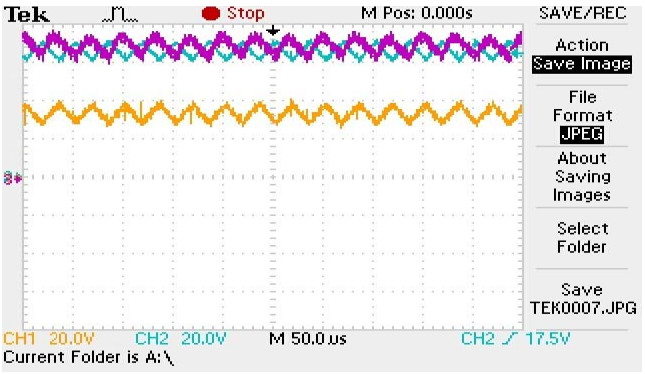



Fig.14. Variable interleaved method output dc voltages

completely eliminated. In Fig.10 the variable interleaving is implemented and, as it is demonstrated the DC link voltage ripple becomes very small and is approximately removed. Fig. 11 shows the DC Link voltage FFT analysis. As it is illustrated the first harmonic component of the DC output voltage is completely eliminated.

## IV. TECHNIQUES HARDWARE-IN-THE-LOOP- TEST

A Hardware-in-the-Loop test has been done to verify the performance of the algorithm. Exactly the same test system used for PSCAD simulation has been emulated in the Typhoon HIL (Hardware-in-the-Loop testing equipment) [15]. The converter firing signals (Fs=30 kHz) are being generated in an external controller which is properly interfaced with Typhoon HIL via an interface board as shown in Fig. 12. Fig.13, 14 and 15 demonstrate the DC link output voltage with two Fixed and one variable interleaving algorithm.

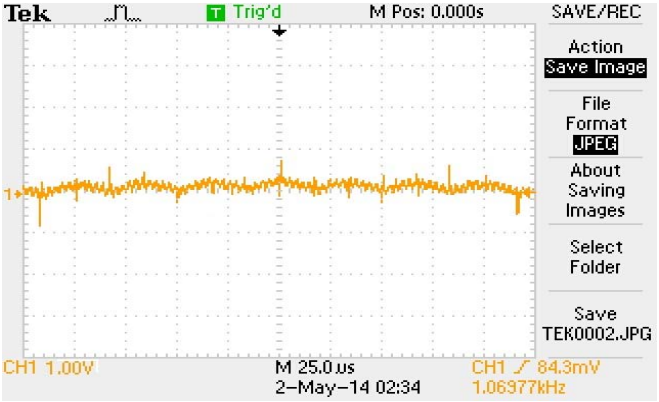



Fig.15. Output dc voltage with variable interleaving algorithm

## V. CONCLUSION

In this study, a variable interleaving technique has been analyzed for cascaded DC/DC converters in PV application. The cascaded rather than parallel connection of DC/DC converters allows the input-output voltage to be close to unity which leads to low voltage switches, diodes, inductors and capacitors. Efficiencies are close to 99% and converters can be small, light and low cost. However; under inhomogeneous irradiation, the power generated by each PV module and the output DC voltage become unbalanced.

The goal is to minimize the DC link voltage ripple and consequently reduce the required DC link capacitance in cascaded systems under an asymmetric condition. The same issue for parallel connections was first addressed in [8] and a new variable interleaving algorithm has been employed, studied and extended to the cascaded DC/DC converters for PV applications under asymmetric condition. It has been shown that the variable interleaving technique has good performance in eliminating the DC link voltage ripple in case of asymmetry.

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