A Control Scheme for PWM Voltage-Source Distributed-Generation Inverters for Fast Load-Voltage Regulation and Effective Mitigation of Unbalanced Voltage Disturbances

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***Abstract*—This paper presents a control scheme for grid-connected pulsewidth-modulated voltage-source inverters (VSIs) featuring fast load-voltage regulation and effective mitigation of unbalanced voltage disturbances. To ensure perfect regulation of the voltage at the point of common coupling (PCC) and provide means for rejecting fast and dynamic voltage disturbances, the frequency modes of the disturbances to be eliminated should be included in the stable closed-loop system. Toward this, a hybrid voltage controller combining a linear with variable-structure control element is proposed for an inverter-based distributed-generation interface to regulate the voltage at the PCC. The proposed voltage controller can embed a wide band of frequency modes through an equivalent internal model. Subsequently, a wide range of voltage perturbations, including capacitor-switching disturbances, can be rejected. To account for unbalanced voltage disturbances, a dual-sequence voltage controller is proposed. To provide accurate and robust tracking of the generated active and reactive current trajectories, a newly designed deadbeat current control algorithm is proposed. The controller is designed under the practical considerations of inherent plant delays, which are associated with the digital implementation of the control algorithm, and the uncertain nature of the current dynamics. Theoretical analysis and comparative evaluation tests are presented to demonstrate the effectiveness of the proposed control scheme.**

***Index Terms*—Deadbeat current control, fast load-voltage regulation, grid-connected inverters, pulsewidth-modulated (PWM) inverters.**

I. Introduction

FAST load-voltage regulation is a necessary requirement in a power distribution system, particularly in feeders serving voltage-sensitive loads. Severe and random voltage disturbances might be initiated by time-varying loads, such as arc furnaces [1]; nondispatchable generation, such as the fluctuating output power of wind and photovoltaic generation [2], [3]; voltage transients associated with parallel connected loads, such as line-start induction motors [4]; and voltage transients caused by capacitor switching [5]. These voltage disturbances are stochastic in nature, with durations that vary from a fraction of a cycle to a few cycles.

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Recently, controlled reactive power sources, such as distribution static synchronous compensators (DSTATCOMs) [6], [7], active power filters (APFs) [8], and inverter-based distributed generation (DG) [9], are proposed for load-voltage regulation at the point of common coupling (PCC). In these applications, three-phase pulsewidth-modulated (PWM) current-controlled voltage-source inverters (CC-VSIs) are commonly used, whereas the control algorithm is realized using the axis theory for balanced three-phase systems. In typical operation of these custom power devices, a reactive reference current is generated from a voltage controller to regulate the load bus voltage, and an internal current control loop is used to regulate the output current. However, existing voltage regulation techniques yield a relatively slow regulation performance. Typical voltage-recovery times in the range of 0.005–0.06 s with voltage dips of about 0.1–0.4 p.u. are reported [6]–[9]. With these figures, the voltage regulation performance might not be fast enough for voltage-sensitive loads. More importantly, existing voltage regulation schemes cannot mitigate fast voltage disturbances in the subcycle range, such as capacitor switching transients. A control structure for controlled reactive power sources capable of fast voltage regulation and effective mitigation of fast voltage disturbances demands special attention.

Generally, voltage regulation design in shunt-type custom power devices, such as DSTATCOM, APF, and inverter-based DG, is twofold: 1) voltage control loop design and 2) current control loop design. Considering the voltage control loop, several control methods have been reported. Conventionally, proportional–integral (PI) controllers have been used to generate the reactive current component [7]. However, these linear controllers are working against nonlinear error dynamics. In addition, there is difficulty in designing these controllers to regulate the fundamental frequency voltage and reject higher frequency disturbances. PI regulators with their pole at zero-frequency cannot achieve fast voltage regulation and certainly cannot mitigate fast voltage disturbances. Similar observations can be found in [8], where a PI-based voltage controller has been added to the APF to regulate the voltage at the PCC. In [6], a nonlinear control based on feedback regulation of system states to the reference values, which are statically related to the reference phase voltage magnitude through system parameters, is proposed for a DSTATCOM. However, the method is complex and requires system parameter adaptation. In addition,

the voltage dip due to load disturbance is large, i.e., about 0.3 p.u. with a recovery time of about 5 ms. In [9], the DG interface is designed with a fuzzy-logic-based voltage controller to handle the nonlinearity of the voltage control loop. However, the voltage regulation response is sluggish, with a recovery time of about 0.05 s. To ensure perfect regulation of the voltage at the PCC and provide means for rejecting voltage disturbances, the frequency modes of the disturbances to be eliminated should be included in the stable closed-loop system. At this condition, the tracking error will not contain these frequency modes. This criterion is satisfied if the voltage controller can supply an internal model [10]. Neither a linear controller nor a nonlinear controller can reject a wide band of voltage disturbances unless an internal model for the voltage disturbances is provided. For periodic disturbances, the repetitive control approach can be applied for voltage regulation [11]. However, voltage disturbances are not periodic by nature. Moreover, the repetitive control is not easy to stabilize for all unknown disturbances and cannot attain very fast response. To overcome the aforementioned difficulties, a variable-structure control (VSC) approach is proposed to design the voltage controller. In the case where the perturbations are random and nonperiodic, VSC perhaps is the best solutions when high performance is required. Moreover, the VSC is well suited for nonlinear dynamic systems with uncertainties [12]. In the VSC approach, a discontinuous fast switching control law forces an infinite gain at the equilibrium point. Subsequently, a wide band of frequency modes are supplied through an equivalent internal model. By this technique, a wide range of voltage perturbations can be rejected. However, the VSC approach has practical limitations, such as chattering and nonlinear sliding motion effects, which arise from the extremely high gain around the equilibrium and the limited switching frequency. Subsequently, not all the frequency modes can be rejected in a practical VSC. In addition, the chattering effect might counteract the power quality requirements imposed on the injected power. Therefore, a hybrid voltage controller combining a linear with VSC element and switching function approximation is proposed and applied to an inverter-based DG interface to regulate the voltage at the PCC. The hybrid voltage control law gives more degrees of freedom to achieve adequate control performance with enough robustness against fast voltage disturbances with reduced chattering.

A current control loop with high-bandwidth characteristics is necessary to allow accurate tracking of the highly dynamic reference trajectory generated by the voltage controller.[1] The major techniques to regulate the output current of a CC-VSI include either a variable-switching frequency, such as the hysteresis control scheme, or fixed-switching frequency schemes, such as the ramp comparison, stationary and synchronous frame PI, and deadbeat predictive current control schemes [13]. Hysteresis-based schemes give fast transient response; however, they are documented to suffer from interphase distortion, the possible existence of undesirable limit cycle behavior, and poor steady-state performance with errors of up to twice the hysteresis band when the load neutral is isolated. Moreover, they result in unpredictable average converter switching frequency that varies with the load parameters, and consequently, the load current harmonics ripple is not optimal. Even though some methods are reported to constrain the variations in switching frequency [14], [15], the incompatibility with fully digital platforms and the additional complexity make this scheme far from being practical. Ramp comparison control using a PI regulator in the stationary frame has a long history of use; however, it has the disadvantages of steady-state phase errors and sensitivity to system parameters. Resonant stationary-frame controllers have been proposed to null the phase errors [16]–[18]; however, resonant controllers provide internal model dynamics at preset frequency modes, and the tuning process of these controllers is not straightforward [18]. By using the synchronous rotating frame [19], [20], the PI regulator can be used without the phase lag associated with stationary-frame PI regulators. However, this scheme does not achieve optimal dynamic response from the converter due to its relatively slow transient response and the nondefined robustness properties. Currently, there is a strong trend toward fully digital control of power converters based on deadbeat current control techniques [21]–[28], which offer the potential for achieving the fastest transient response, more precise current control, zero steady-state error, and full compatibility with digital control platforms. Moreover, when combined with the space vector modulation (SVM) technique, this control scheme is known to provide the lowest distortion and the lowest current ripples [22]. However, there are two main practical issues that are related to the deadbeat current control: 1) bandwidth limitation due to the inherent plant delay and 2) sensitivity to variations in the current loop parameters [27]. An adaptive self-tuning deadbeat current controller that overcomes these issues has been developed by Mohamed and El-Saadany [29]. A newly designed deadbeat current control algorithm, based on robust modeling and uncertainty estimation, is proposed in this paper. The deadbeat current controller employs a simple delay compensation method, which forces the delay elements, which are caused by voltage calculation, PWM, and synchronous frame rotation, to be equivalently placed outside the closed-loop control system. Hence, their effect on the closed-loop stability is eliminated, and the current controller can be designed with a higher bandwidth. To guarantee the robustness and stability of the deadbeat current controller, an adaptive uncertainty observer is emerged in the current control structure to achieve a robust current regulation performance. In addition, the predictive nature of the uncertainty observer has the necessary phase advancement to compensate for system delays.

The remainder of this paper is organized as follows. In Section II, modeling of a three-phase voltage-oriented CC-VSI is presented. In Section III, the proposed control system is described. Evaluation results are provided in Section IV. Conclusions are drawn in Section V.

II. Modeling of a Voltage-Oriented CC-VSI

Fig. 1 shows a network connection of a grid-connected VSI used to interface a DG unit, where R and L represent the

[1] If the current control loop is designed to offer a very fast step response, arbitrary trajectory tracking can be feasible.

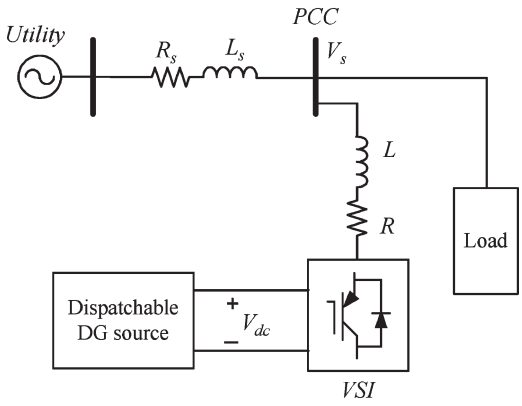

Fig. 1. Network connection of a VSI with DG.

equivalent resistance and inductance of the ac filter, coupling transformer (if any), and connection cables, respectively; R_s and L_s represent the feeder resistance and inductance up to the PCC, respectively; v_s is the supply voltage at the PCC; and $V_{\rm dc}$ is the dc-link voltage.

Using the voltage-oriented control, the active and reactive power injections can be controlled via a CC-VSI. To impose an arbitrary current in the inductive coupling impedance, a current controller is usually adopted to shape the voltage applied on the inductor, so that minimum current error is achieved. An outer power/voltage control loop can be used to generate the reference current vector.

In Park's $d-q$ frame that synchronously rotates with the grid angular speed ω, the current dynamics can be reasonably represented by the following equations:

$$v_q = Ri_q + L\frac{di_q}{dt} + L\omega i_d + v_{sq} \tag{1}$$

$$v_d = Ri_d + L\frac{di_d}{dt} - L\omega i_q + v_{sd} \tag{2}$$

where v_d, v_q, i_d, and i_q are the d- and q-axis inverter's voltages and currents, respectively; L is the coupling inductance; R is the coupling resistance; and v_{sd} and v_{sq} are the d- and q-axis components of the supply voltage at the PCC.

The injected active and reactive power components p and q can be represented in terms of the d- and q-axis components of the supply voltage at the PCC and the injected currents as follows:

$$p = \frac{3}{2}(v_{ds}i_d + v_{qs}i_q) \tag{3}$$

$$q = \frac{3}{2}(v_{qs}i_d - v_{ds}i_q). \tag{4}$$

In addition, the magnitude of the voltage at the PCC is given by

$$|v_s| = \sqrt{v_{sd}^2 + v_{sq}^2}. \tag{5}$$

Considering the physical constraints, the preceding model is subjected to the following limits: The injected current is limited to the maximum continuous current of the inverter or to the maximum available current of the inverter in a limited short-time operation. In addition, the load voltage is limited to the maximum available output voltage of the inverter, depending on the dc-link voltage.

Since the distribution system is uncertain and dynamic in nature and its parameters frequently vary due to factors such as cable overload, transformer saturation, and temperature effects, the uncertainty in system parameters should be considered in the control system design.

Using the nominal system parameters and considering the grid voltage components as a dynamic disturbance, (1) and (2) can be rewritten as follows:

$$v_q = R_o i_q + L_o\frac{di_q}{dt} + L_o\omega i_d + f_q \tag{6}$$

$$v_d = R_o i_d + L_o\frac{di_d}{dt} - L_o\omega i_q + f_d \tag{7}$$

where the subscript "o" denotes the nominal value; and f_q and f_d represent the lump of uncertainties, which are caused by parameter variations, current loop disturbances, and other unstructured uncertainties, and are given by

$$f_q = \Delta R i_q + \Delta L\frac{di_q}{dt} + \Delta L\omega i_d + v_{sq} + n_q \tag{8}$$

$$f_d = \Delta R i_d + \Delta L\frac{di_d}{dt} - \Delta L\omega i_q + v_{sd} + n_d \tag{9}$$

where $R = R_o + \Delta R$, $L = L_o + \Delta L$, and n_q and n_d, represent unstructured uncertainties due to unmodeled dynamics.

The current dynamics in (6) and (7) can be represented by the following state space equations:

$$\dot{\boldsymbol{x}} = \boldsymbol{A_{co}x} + \boldsymbol{B_{co}u} + \boldsymbol{G_{co}f} \quad \boldsymbol{y} = \boldsymbol{Cx} \tag{10}$$

with

$$\boldsymbol{x} = [\,i_q \quad i_d\,]^T, \boldsymbol{u} = [\,v_q - \omega L_o i_d \quad v_d + \omega L_o i_q\,]^T,$$

$$\boldsymbol{f} = [\,f_q \quad f_d\,]^T, \boldsymbol{A_{co}} = \begin{bmatrix} -R_o/L_o & 0 \\ 0 & -R_o/L_o \end{bmatrix},$$

$$\boldsymbol{B_{co}} = \begin{bmatrix} 1/L_o & 0 \\ 0 & 1/L_o \end{bmatrix}, \boldsymbol{G_{co}} = \begin{bmatrix} -1/L_o & 0 \\ 0 & -1/L_o \end{bmatrix},$$

$$\boldsymbol{C} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

where $\boldsymbol{A_{co}}$, $\boldsymbol{B_{co}}$, and $\boldsymbol{C}$ are the nominal system matrices of a continuous-time system; and $\boldsymbol{u}$ is the equivalent control input vector.

In the case of slow and small voltage perturbations, the nonlinearity of the voltage control problem is limited, and a linear voltage regulator can be synthesized in the sense of the small-signal model. However, for fast and large voltage disturbances, the nonlinear nature of the voltage dynamics cannot be neglected, and the voltage controller should be synthesized in the sense of the large signal dynamics of the voltage control loop. Other control system nonlinearities are associated with the inverter system operation and control, such as the

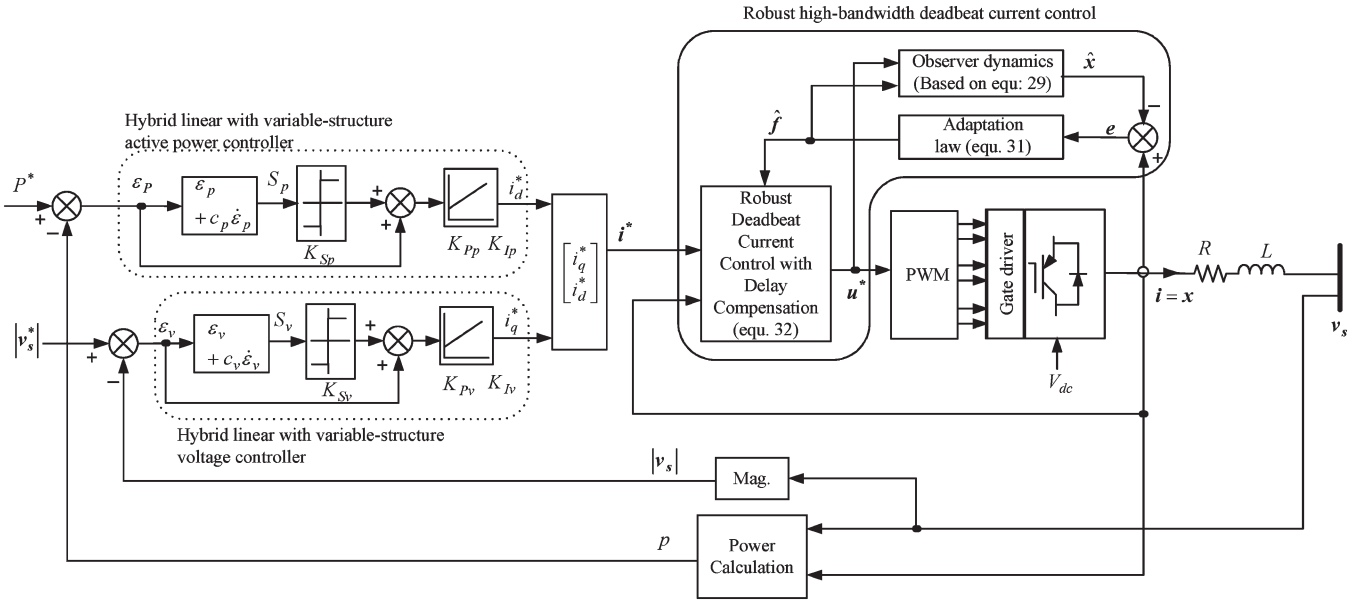

Fig. 2. Proposed control scheme.

dead-time effect, device voltage drop, current loop and PWM limits, dc-link ripples, coupling dynamics between the active and reactive power components, and imperfect measurements.

III. Control System Development

Fig. 2 shows the block diagram of the proposed control scheme for a grid-connected DG-based VSI. To achieve a fast voltage regulation performance with the capability of mitigating fast voltage disturbances, a hybrid voltage controller combining the linear control and the VSC approach is proposed to generate the reactive current reference. As an inherent feature of the VSC, the controller can introduce an infinite gain at equilibrium, leading to high disturbance-rejection performance. To achieve a robust active power control performance, a power controller employing the hybrid linear with VSC structure is proposed to generate the active current reference. The invariance property to system uncertainties in the sliding mode enhances the robustness against the active and reactive power coupling dynamics. To track the dynamic reference current trajectories generated by the voltage and power controllers, a newly designed high-bandwidth current controller, based on the deadbeat control technique, is proposed. The current controller is designed to achieve deadbeat response and to offer enough robustness against current loop uncertainties. The SVM technique is used to synthesize the control voltage vector calculated by the deadbeat current controller.

A. Voltage and Power Control

The main objective of the voltage and power controller is to achieve fast and accurate generation of the reactive and active current references. To achieve this objective, two linear with variable-structure controllers are adopted, as shown in Fig. 2. In the VSC strategy, a switching control law is used to drive the plant's state trajectory onto a chosen surface in the state space (sliding surface). In the present design problem, the sliding surfaces are selected to achieve first-order dynamics for the sliding-mode operation as follows:

$$S_v = \varepsilon_v + c_v \frac{d\varepsilon_v}{dt} \tag{11}$$

$$S_p = \varepsilon_p + c_p \frac{d\varepsilon_p}{dt} \tag{12}$$

where $\varepsilon_v = |v_s^*| - |v_s|$ and $\varepsilon_p = p^* - p$ are the voltage and power control errors, respectively; c_v and c_p are the coefficients of the sliding surface; and the symbol "$*$" denotes the reference value.

In the sliding mode, it is required to restrict the controlled states onto their corresponding sliding surfaces. This is exclusively governed by $S_v = \dot{S}_v = 0$ and $S_p = \dot{S}_p = 0$. At this condition, the equivalent dynamics can be described as

$$\varepsilon_v = -c_v \frac{d\varepsilon_v}{dt} \tag{13}$$

$$\varepsilon_p = -c_p \frac{d\varepsilon_p}{dt}. \tag{14}$$

The sliding surface coefficients can be chosen to achieve the required dynamic performance on the sliding surface.

In order to increase the degrees of freedom in tuning the controller, the following linear with VSC inputs are used:

$$i_q^* = \left(K_{Pv} + \frac{K_{Iv}}{s}\right)(\varepsilon_v + K_{Sv}\mathrm{sgn}(S_v)) \tag{15}$$

$$i_d^* = \left(K_{Pp} + \frac{K_{Ip}}{s}\right)(\varepsilon_p + K_{Sp}\mathrm{sgn}(S_p)) \tag{16}$$

where s is the Laplace operator; K_{Pv}, K_{Iv}, K_{Pp}, and K_{Ip} are the gains of the PI part of the control law; and K_{Sv} and

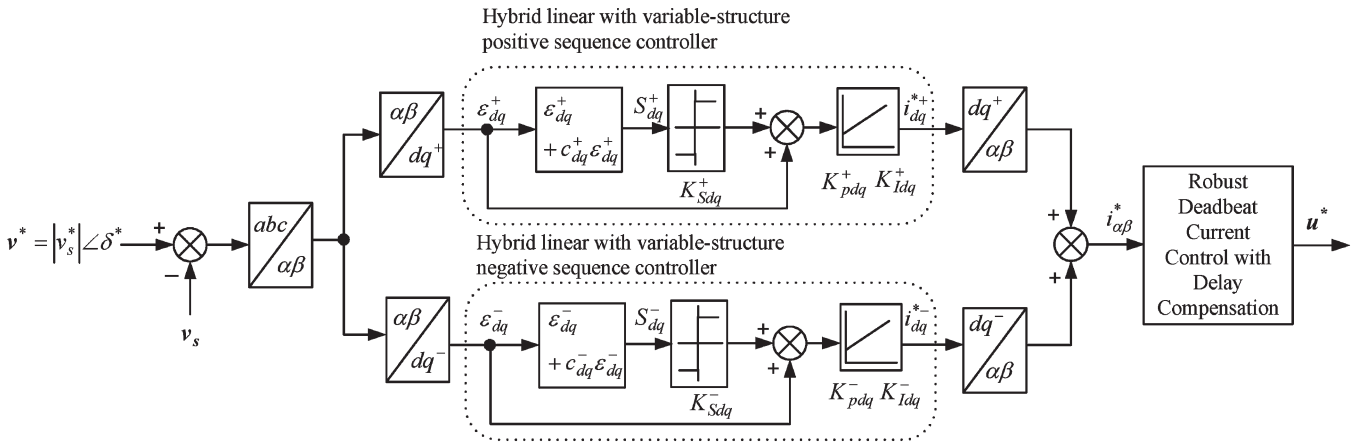

Fig. 3. Proposed control structure for unbalanced grid voltage regulation.

K_{Sp} are the switching gains of the VSC. The control laws in (15) and (16) employ a linear PI controller with a variable-structure controller in a parallel structure. This configuration has a dual behavior by generating a switching excitation signal, which is superimposed by a smooth linear control effort and the slow motion integral of the switching signal. It is clear that the VSC behavior can be controlled by gains K_{Sv} and K_{Sp}, whereas the linear control behavior is controlled by gains K_{Pv}, K_{Iv}, K_{Pp}, and K_{Ip}. The control laws in (15) and (16) restrict the system states onto the surfaces S_v and S_p in the sliding mode. In addition, they give more degrees of freedom to achieve adequate control performance with high robustness.

Since the PI part independently operates on the variable-structure part, the PI control element can be tuned to yield a specific tracking performance, whereas the VSC element can be tuned to yield a high disturbance rejection performance. Generally, the VSC design procedure requires the switching gains to be large enough to achieve wideband disturbance rejection. However, under steady-state conditions, the voltage tracking error will be close to zero. Under this condition, the VSC will be very sensitive to any noise in the tracking error, and control chattering will be yielded. However, the chopped control effort at the steady-state condition can be suppressed by approximating the switching function $\mathrm{sgn}(S(t))$ by $S(t)/(|S(t)|+r)$, where r is given by

$$r = \begin{cases} 0, & |S(t)| \geq \delta \\ \lambda, & |S(t)| < \delta \end{cases} \tag{17}$$

where λ is a large positive value, and δ is a small positive constant. The values of λ and δ can be selected in a tradeoff between the robustness and the chattering performance. Practically, adequate performance can be obtained by using this approximation.

The aforementioned voltage regulation scheme takes into account only the positive-sequence case. However, the uneven distribution of single-phase loads and the diversity in their demands give rise to mild voltage unbalance. In other cases, severe short-tem unbalances can be yielded in the case of system faults. The direct result of these unbalances is additional losses, and performance degradation of line-start motors, motor drives, and power-electronic converters. Therefore, the voltage regulation scheme should incorporate a negative-sequence regulator. The proposed voltage control scheme can be extended to mitigate grid voltage unbalance by adding a negative-sequence regulator. Fig. 3 depicts the proposed control structure for unbalanced grid voltage regulation. The actual grid voltage vector is compared to the reference grid voltage vector. The voltage vector control error is projected onto positive- and negative-sequence synchronous frames using filtered forward- and reverse-rotating synchronous frames, which are denoted by dq^+ and dq^-, respectively. The positive-sequence error vector ε^+_{dq} is processed by a hybrid variable-structure positive-sequence controller to generate the positive-sequence reference current vector i^{*+}_{dq}. Similarly, the hybrid variable-structure negative-sequence controller generates the negative-sequence reference current vector i^{*-}_{dq} using the negative-sequence error vector ε^-_{dq}. A deadbeat current control scheme is utilized to impose the total reference current in the coupling-filter inductive winding.

B. Current Control

A fast current control loop is necessary to allow fast tracking of the reference current trajectories and to allow the VSI to act as a current amplifier within the current loop bandwidth. This section presents a deadbeat current control system, which allows fast transient response and a transient-following tracking operation. The controller is designed under the practical considerations of inherent plant delays, which are associated with the digital implementation of the control algorithm, and the uncertain nature of the current dynamics.

Since the harmonic components included in the inverter's output voltage are not correlated with the sampled reference currents, the PWM VSI can be considered as a zeroth-order hold circuit with a transfer function $H(s)$ given by

$$H(s) = \frac{1 - e^{-sT}}{s} \tag{18}$$

where T is the discrete-time control sampling period, and s is the Laplace operator.

For the digital implementation of the control algorithm, the current dynamics in (10) can be represented in a discrete-time domain with the conversion $H(s)$ in (18) as follows:

$$\boldsymbol{i}(k+1) = \boldsymbol{A_o}\boldsymbol{i}(k) + \boldsymbol{B_o}\boldsymbol{u}(k) + \boldsymbol{G_o}\boldsymbol{f}(k) \tag{19}$$

where

$$\boldsymbol{i}(k) = [\, i_q(k) \quad i_d(k) \,]^T \quad \boldsymbol{f}(k) = [\, f_q(k) \quad f_d(k) \,]^T$$
$$\boldsymbol{u}(k) = [\, v_q(k) - \omega L_o i_d(k) \quad v_d(k) + \omega L_o i_q(k) \,]^T$$

and $\boldsymbol{A_o}$ and $\boldsymbol{B_o}$ are the nominal sampled equivalents of the continuous-time system matrices. If the continuous system in (10) is sampled with interval T, which is at least ten times shorter than the load time constant, then the matrices of the discrete-time system $\boldsymbol{A_o}$, $\boldsymbol{B_o}$, and $\boldsymbol{G_o}$ can be obtained by Euler's approximation as follows:

$$\boldsymbol{A_o} = \begin{bmatrix} 1 - \frac{TR_o}{L_o} & 0 \\ 0 & 1 - \frac{TR_o}{L_o} \end{bmatrix} \quad \boldsymbol{B_o} = \begin{bmatrix} \frac{T}{L_o} & 0 \\ 0 & \frac{T}{L_o} \end{bmatrix}$$
$$\boldsymbol{G_o} = \begin{bmatrix} -\frac{T}{L_o} & 0 \\ 0 & -\frac{T}{L_o} \end{bmatrix}. \tag{20}$$

Assuming that the lump of uncertainties $\boldsymbol{f}(k)$ is known and using the discrete-time dynamics in (18), the conventional deadbeat current controller [21] can be realized by the following control effort:

$$\boldsymbol{u}^*(k) = \boldsymbol{B_o}^{-1}\{\boldsymbol{i}^*(k+1) - \boldsymbol{A_o}\boldsymbol{i}(k) - \boldsymbol{G_o}\boldsymbol{f}(k)\} \tag{21}$$

where the subscript "$*$" denotes reference values.

The control law in (21) does not account for system delays by assuming that the control period is much longer than the calculation time of (21). Practically, when the control period is chosen to be small, inherent and nonnegligible delays that are associated with the implementation of the digital control scheme reduce the stability margins, particularly when high feedback gains are used. On the other hand, if the delay effect is appropriately compensated, the bandwidth criterion is relaxed. In fact, the compensation of the time delay significantly increases the current controller bandwidth without increasing the inverter's switching frequency.

In order to enhance the bandwidth characteristics, in the presence of system delays, a delay compensation method is adopted in this paper. During the $(k+1)$th period of the control process, the current is forced by the control voltage $\boldsymbol{u}(k+1)$, which is calculated in the kth period. The resultant current, which is sensed at the beginning of the $(k+2)$th period, can be given by

$$\boldsymbol{i}(k+2) = \boldsymbol{A_o}\boldsymbol{i}(k+1) + \boldsymbol{B_o}\boldsymbol{u}(k+1) + \boldsymbol{G_o}\boldsymbol{f}(k+1). \tag{22}$$

It is obvious that current vector $\boldsymbol{i}(k+2)$ is affected by current vector $\boldsymbol{i}(k+1)$ and control voltage $\boldsymbol{u}(k+1)$. By using current vector $\boldsymbol{i}(k+1)$, current vector $\boldsymbol{i}(k+2)$ can be given by

$$\boldsymbol{i}(k+2) = \boldsymbol{A_o}\left(\boldsymbol{A_o}\boldsymbol{i}(k) + \boldsymbol{B_o}\boldsymbol{u}(k) + \boldsymbol{G_o}\boldsymbol{f}(k)\right) + \boldsymbol{B_o}\boldsymbol{u}(k+1) + \boldsymbol{G_o}\boldsymbol{f}(k+1). \tag{23}$$

For current regulation, current vector $\boldsymbol{i}(k+2)$ can be regarded as the reference current vector. Accordingly, the appropriate control voltage can be predictably obtained as

$$\boldsymbol{u}^*(k+1) = \boldsymbol{B_o}^{-1}\{\boldsymbol{i}^*(k+2) - \boldsymbol{A_o}\left(\boldsymbol{A_o}\boldsymbol{i}(k) + \boldsymbol{B_o}\boldsymbol{u}(k) + \boldsymbol{G_o}\boldsymbol{f}(k)\right) - \boldsymbol{G_o}\boldsymbol{f}(k+1)\}. \tag{24}$$

According to (24), the control voltage can be calculated with the measured quantities at the kth sample, and the two-sample delay is equivalently removed outside the closed-loop control to appear in the two-step-ahead reference current vector. Assuming known uncertainty dynamics $\boldsymbol{f}$ (this assumption will be relaxed later by adopting a high bandwidth uncertainty estimator) and using (24) with the current dynamics in (18), the output current vector can be given as

$$\boldsymbol{i}(k) = \boldsymbol{i}^*(k-2). \tag{25}$$

Accordingly, the frequency response of the reference-to-output transfer function matrix is

$$\boldsymbol{T}(e^{j\omega T}) = \begin{bmatrix} e^{-2j\omega T} & 0 \\ 0 & e^{-2j\omega T} \end{bmatrix} \tag{26}$$

which has a unity gain, and a phase lag corresponds to the two-sampling-period delay, which are equivalently removed outside the closed loop to appear in the reference side. To compensate for this delay, the forward estimate of the reference current vector is necessary. This equivalently works as adding an equal and opposite phase shift to the reference trajectory. The reference current vector can be predicted via linear extrapolation as follows:

$$\boldsymbol{i}^*(k+2) = 3\boldsymbol{i}^*(k) - 2\boldsymbol{i}^*(k-1). \tag{27}$$

With the aforementioned control sequence, the synchronous frame rotates, and there will be a position difference between the kth and the $(k+1)$th interrupt times. Since the control voltage is applied during the $(k+1)$th period, the position difference can be adjusted by averaging the reference frame position over one switching period. Therefore, the corrected voltage command can be given in the following space vector form:

$$\vec{\boldsymbol{u}}^*(k+1) = \boldsymbol{u}^*(k+1)e^{j(2.5\theta(k) - 1.5\theta(k-1))} \tag{28}$$

where $\theta(k)$ is the synchronous frame position at the current sampling period, and it is obtained via a dq-phase-locked loop [30].

As shown in (24), robust control voltage generation can be achieved if the uncertainty dynamics $\boldsymbol{f}$ is known. However, in practical applications, the grid voltage and system parameters R and L are subjected to considerable uncertainties. This paper presents a robust deadbeat current control technique. The robust controller is realized, with low computational demand, by including an adaptive internal model for the estimated uncertainty dynamics within the current feedback structure. The inclusion of the estimated uncertainty dynamics provides an efficient solution for attenuating the effects of the current loop disturbances; hence, accurate current tracking can be yielded. Furthermore, the proposed robust controller utilizes the one-step-ahead uncertainty dynamics $\boldsymbol{f}(k+1)$, which can be robustly predicted, as shown here. The predictive nature of the proposed estimator has the necessary phase advance of the estimated disturbance, which compensates for the system's delays.

To estimate unknown uncertainty dynamics $\boldsymbol{f}$, let us construct an adaptive natural observer with the following input/output relation:

$$\dot{\hat{\boldsymbol{x}}} = \boldsymbol{A_{co}}\hat{\boldsymbol{x}} + \boldsymbol{B_{co}}\boldsymbol{u} + \boldsymbol{G_{co}}\hat{\boldsymbol{f}} \tag{29}$$

where the subscript "∧" denotes estimated values.

Assuming that the nonlinearities associated with the inverter operation—particularly the blanking time and the voltage limitation effects—are properly compensated, the actual voltage components can be replaced with the reference ones, in (29). This assumption is justified by considering that the inverter's switching period is much smaller than the circuit time constant. As a result, the direct measurements, which are affected by the modulation and acquisition noise, are avoided.

Under the same input voltage and disturbance, the estimated state vector approaches the actual state vector. Therefore, convergence of the proposed observer can be achieved with an appropriate disturbance voltage adaptation using estimation error $\boldsymbol{e} = [\, e_{iq} \quad e_{id}\,]^T \equiv \boldsymbol{x} - \hat{\boldsymbol{x}}$. Using (10) and (29), the following error dynamics can be obtained:

$$\dot{\boldsymbol{e}} = \boldsymbol{A_{co}}\boldsymbol{e} + \boldsymbol{G_{co}}\tilde{\boldsymbol{f}} \tag{30}$$

where $\tilde{\boldsymbol{f}} = \boldsymbol{f} - \hat{\boldsymbol{f}}$ is the uncertainty estimation error vector. For nominal system parameters, matrix $\boldsymbol{A_{co}}$ is Hurwitz. In addition, the damping rate of $\boldsymbol{A_{co}}$ can be easily controlled by adding a feedback gain matrix for the estimation error. As a result, according to the Lyapunov equation [31], there exist $\boldsymbol{P} = \boldsymbol{P}^T$ and $\boldsymbol{Q} > 0$ such that $\boldsymbol{A}_{\boldsymbol{co}}^T\boldsymbol{P} + \boldsymbol{P}\boldsymbol{A_{co}} = -\boldsymbol{Q}$. The disturbance adaptation rule can be derived in the sense of the Lyapunov stability theory as [derivation can be found in Appendix A]

$$\dot{\hat{\boldsymbol{f}}} = \eta \boldsymbol{G}_{\boldsymbol{co}}^T\boldsymbol{P}\boldsymbol{e} \tag{31}$$

where η is the adaptation gain, and $\boldsymbol{P}$ is the solution of the Lyapunov equation.

To ensure the bounded stability of the proposed adaptive observer, $\hat{\boldsymbol{f}}$ is limited within a range defined by the lower and upper limits $\boldsymbol{f}_{\min}$ and $\boldsymbol{f}_{\max}$.

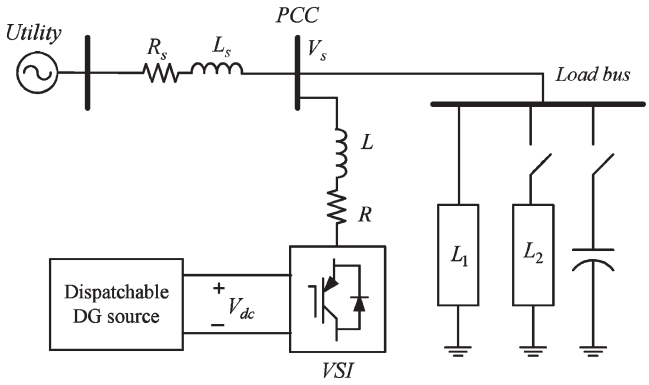

Fig. 4. Test system.

The adaptive estimation law in (31) provides a simple iterative gradient algorithm designed to stabilize (30).

The Euler's approximation method can be adopted to obtain the discrete-time version of the estimator. Accordingly, the estimated uncertainty function can be used to robustly calculate the control voltage as follows:

$$\boldsymbol{u}^*(k+1) = \frac{1}{\beta_o}\left(\boldsymbol{i}^*(k+2) - \alpha_o^2\boldsymbol{i}(k) - \alpha_o\beta_o\left[\boldsymbol{u}(k) - \hat{\boldsymbol{f}}(k)\right]\right) + \hat{\boldsymbol{f}}(k+1) \tag{32}$$

where $\alpha_o = 1 - (TR_o/L_o)$, and $\beta_o = (T/L_o)$.

To achieve higher dc-link voltage utilization and lower distortion in the output current, the SVM technique can be employed to synthesize the control voltage in (32).

The stationary-frame version of the deadbeat controller can be easily derived from (32).

IV. Evaluation Results

To evaluate the performance of the proposed control scheme, a three-phase grid-connected PWM VSI system incorporated with the proposed control scheme, as shown in Fig. 2, has been connected to a test network, as shown in Fig. 4. The system parameters are given in Appendix B. The real-time code of the proposed control scheme is generated by the Real-Time WorkShop, under the Matlab/Simulink environment. The TMS320C30 digital signal processor (DSP) has been chosen as an embedded platform for real-time digital simulation experiments. The execution time of the current control interrupt routine is about 130 μs. Subsequently, a control period $T = 150$ μs is selected. With this setting, a safe central processing unit load coefficient of 86% and a switching frequency of 6.7 kHz have been obtained. As these figures reveal, the processing demand of the proposed control scheme is relatively modest for a DSP system, making it possible to achieve quite high switching frequencies. Since the sharp insulated-gate bipolar transistor commutation spikes may impair the current acquisition process, the synchronous sampling technique with a symmetric SVM module is adopted. With this method, the sampling is performed at the beginning of each modulation cycle. Only two phase currents are fed back as the load neutral is isolated; hence, the third

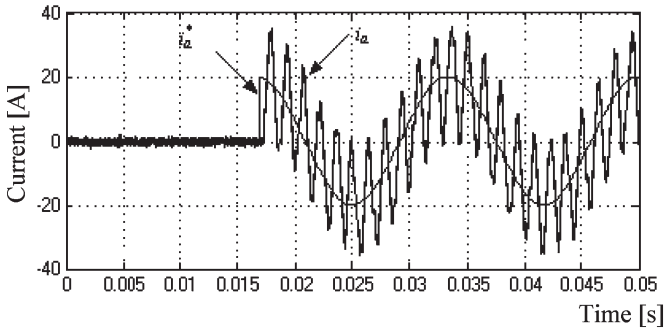

Fig. 5. Performance of the conventional deadbeat current controller implemented in fully digital system.

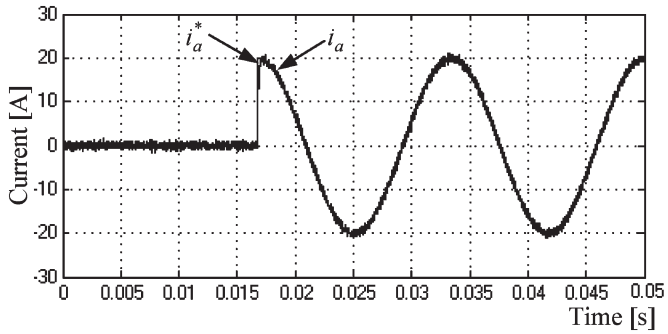

Fig. 6. Performance of the proposed deadbeat current controller implemented in fully digital system.

phase current can be calculated. For the variable-structure voltage and power controllers, the coefficients of the sliding surface are chosen as $c_v = 0.0015$ and $c_p = 0.15$. As a result, the time constant of the S_v and S_p dynamics are set to 1.5 and 150 ms, respectively. The control law parameters are chosen as $K_{Pv} = 0.28$, $K_{Iv} = 380$, $K_{Sp} = 140$, $K_{Pp} = 0.05$, $K_{Ip} = 50$, and $K_{Sp} = 50$. The control parameters are chosen through a numerical search algorithm to achieve appropriate control performance, with consideration of the stability requirements, control effort saturation, and practical operating conditions. The current controller is designed using the following nominal system parameters: $\boldsymbol{A_{co}} = \mathrm{diag}(-400, -400)$, $\boldsymbol{G_{co}} = \mathrm{diag}(400, 400)$, $\eta = 1500$, and $\boldsymbol{Q} = \boldsymbol{I}_{2\times 2}$; therefore, the solution for the Lyapunov equation is $\boldsymbol{P} = \mathrm{diag}(0.00125, 0.00125)$. The bounding limits $\boldsymbol{f}_{\min}$ and $\boldsymbol{f}_{\max}$ are set as $-2|v_s|_{\max}$ and $2|v_s|_{\max}$, respectively, where $|v_s|_{\max}$ is the peak nominal grid voltage.

To verify the feasibility of the proposed controller, different operating conditions have been considered. For the purpose of performance comparison, some selected results are presented here.

A. Current Control Performance

For the sake of performance comparison, the proposed current controller is compared to the conventional deadbeat current controller [21]. Both controllers are tuned using the nominal parameters. The interfacing parameters are set to their nominal values as well. Fig. 5 shows the steady-state performance of the conventional deadbeat current controller in a fully digital system. The d-axis current command is set to 20 A, whereas the q-axis current command is set to 0 A. Since one more period is needed for the control voltage calculation, the conventional deadbeat algorithm leads to sustained oscillations (limit cycles) in the phase-a current response, as shown in Fig. 5. These oscillations and the poor dynamic response are indeed the result of the instability of the control system. In a tradeoff between the bandwidth requirements and the stability, the conventional deadbeat controller should be designed with lower equivalent feedback gains. This negates the deadbeat control performance; therefore, lower control accuracy is yielded.

Fig. 6 shows the current response of the proposed deadbeat controller. The d-axis current command is changed from 0 to 20 A at $t = 0.0167$ s, i.e., a rising step current command, whereas the q-axis current command is set to 0 A. It can be seen that the phase-a current component tracks its reference trajectory precisely with zero steady-state error, zero overshoot, and a rise time of about 250 μs.

To demonstrate the robustness of the proposed deadbeat current control, the proposed controller is compared to the conventional deadbeat control [21] and the robust predictive current controller proposed in [27] under parametric uncertainties. The differences between the performances of the three predictive controllers are due to the delay compensation method and the robustness against current loop uncertainty associated with each controller. Fig. 7 shows the time-domain current responses and the corresponding harmonic spectra of the conventional deadbeat controller, the robust predictive controller in [27], and the proposed controller, respectively. These results are obtained with 60% mismatch in L and 50% mismatch in R; the d-axis current command is set to 20 A, and the q-axis current command is set to 0 A. Fig. 7(a) and (b) shows that the conventional controller is unstable and generates significant low-order harmonics, leading to a total harmonic distortion (THD) of 66.12% up to 8.16 kHz (i.e., up to the 136th harmonic). This result does not meet the IEEE Standard 1547 requirement of THD [32], which is below 5%. Although the predictive controller in [27] is robust up to 53% mismatch in the load inductance, the stability and robustness are remarkably degraded at higher values of uncertainty in the coupling inductance and when the effect of uncertainty in the coupling resistance is considered, as shown in Fig. 7(c). The instability in the current response, combined with the saturation effect of the current controller and PWM limiters, generates low-order harmonics, leading to a THD of 3.37% up to 8.16 kHz, as shown in Fig. 7(d). In contrast, the proposed algorithm is still stable and generates the minimal low-order harmonics even with 60% mismatch in L and 50% mismatch in R, as shown in Fig. 7(e). In this case, the THD up to 8.16 kHz is 0.95%, as depicted in Fig. 7(f).

B. Voltage Control Performance

To evaluate the performance of the proposed interface to compensate for the PCC voltage fluctuation under the condition of a sudden load change, the switched load (L2) is turned on at $t = 0.045$ s. The reference voltage at the PCC is set to 1.0 p.u. Fig. 8 shows the voltage profile without regulation,

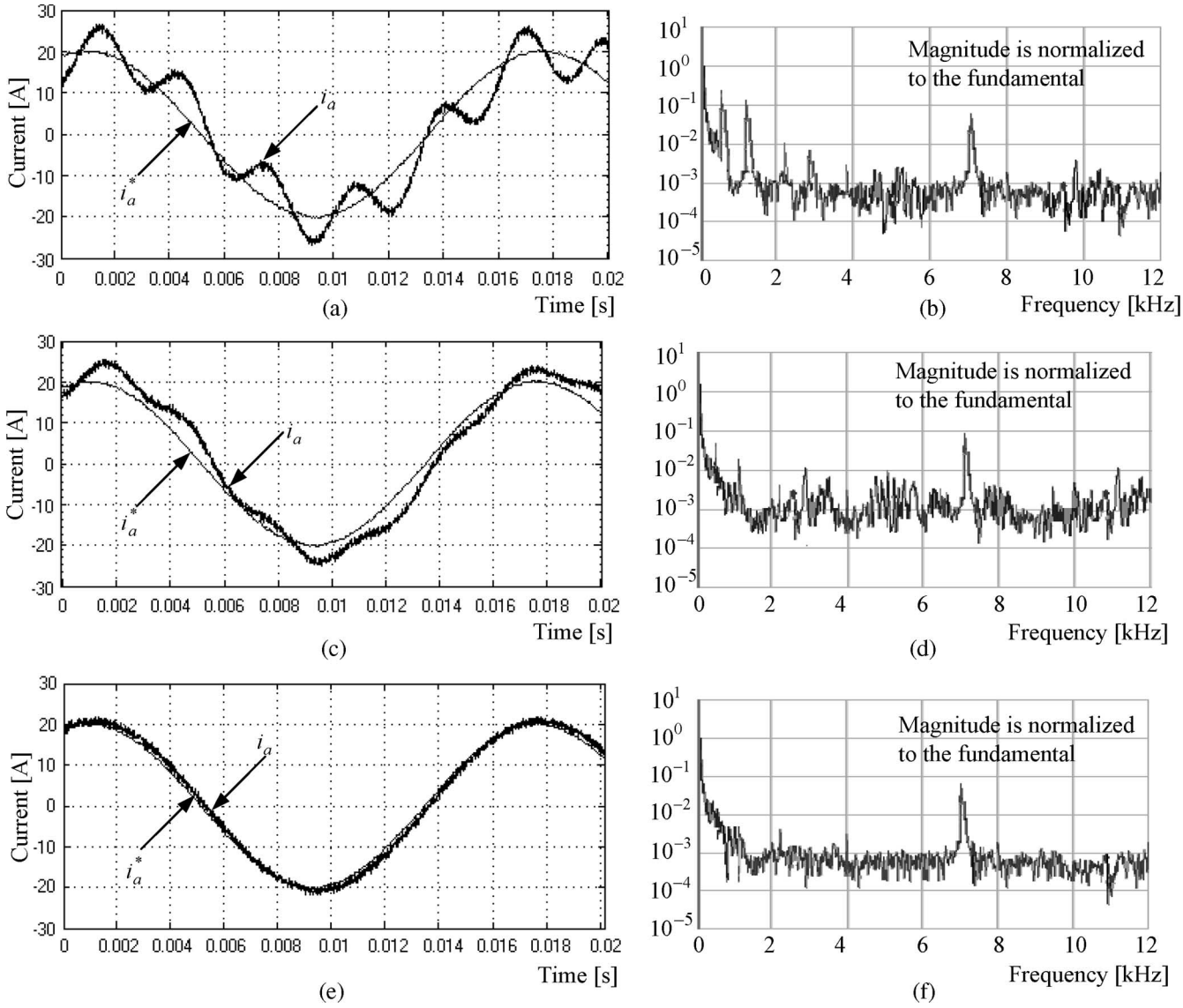

Fig. 7. Performance of the conventional current controller, the robust current controller [27], and the proposed current controller with 60% uncertainty in L and 50% uncertainty in R. (a), (b) Steady-state response and the corresponding harmonic spectrum of the conventional controller. (c), (d) Steady-state response and the corresponding harmonic spectrum of the robust controller proposed in [27]. (e), (f) Steady-state response and the corresponding harmonic spectrum of the proposed controller.

where Fig. 8(a) shows the line-voltage waveform and Fig. 8(b) shows the magnitude of the line voltage at the PCC. Fig. 8 shows that the instantaneous voltage dip is about 0.5 p.u. and the steady-state voltage drop is about 0.15 p.u. Fig. 9 shows the control performance when the proposed voltage regulation scheme is enabled. Fig. 9(a) and (b) shows that the instantaneous voltage dip is less than 0.09 p.u. with a recovery time of about 3 ms. Fig. 9(c) shows the corresponding q-axis current injected to the grid. The reactive current component is quickly generated to regulate the bus voltage and reject the voltage disturbance.

Capacitor switching generates highly dynamic voltage disturbances, which directly impact the voltage quality. Fig. 10(a) and (b) shows the voltage waveform when the capacitor is switched on at $t = 0.045$ s and without voltage regulation. Severe degradation in the voltage quality is yielded by the switching transient. Fig. 11 shows the control performance when the proposed voltage regulation scheme is enabled. Fig. 11(a) and (b) shows that the quality of the voltage waveform is remarkably improved, where most of the transient waveform has been mitigated by the voltage controller. Fig. 11(c) shows the corresponding q-axis current injected to the grid. The reactive current component is quickly generated to regulate the bus voltage and reject the voltage disturbance. The wideband disturbance rejection feature of the variable-structure voltage controller enables effective mitigation of fast and dynamic voltage disturbances, such as the capacitor-switching transients. Fig. 11(d) shows the estimated uncertainty function. It is clear that the proposed uncertainty estimator can track the actual grid voltage disturbance. Therefore, the effect of these disturbances on the current control loop can be mitigated.

To evaluate the voltage regulation performance under unbalanced grid voltage conditions, the proposed dual-sequence voltage controller, which is depicted in Fig. 4, has been tested.

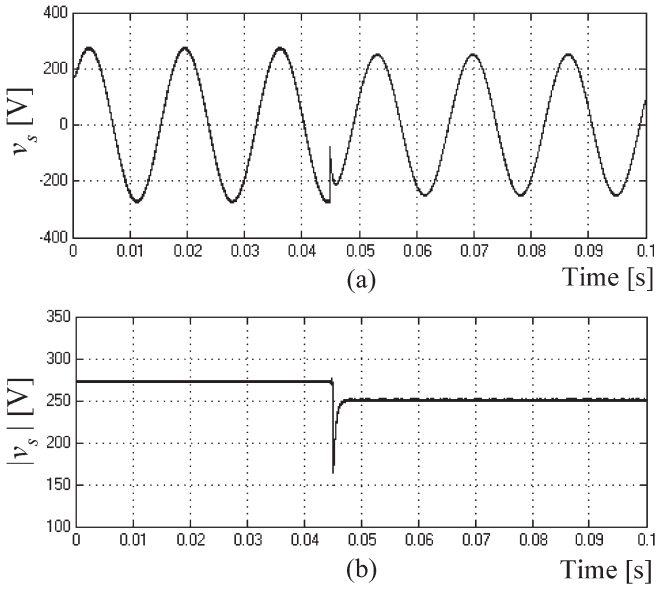

Fig. 8. Voltage drop due to sudden loading of load L2. (a) Voltage waveform. (b) Voltage magnitude at the PCC.

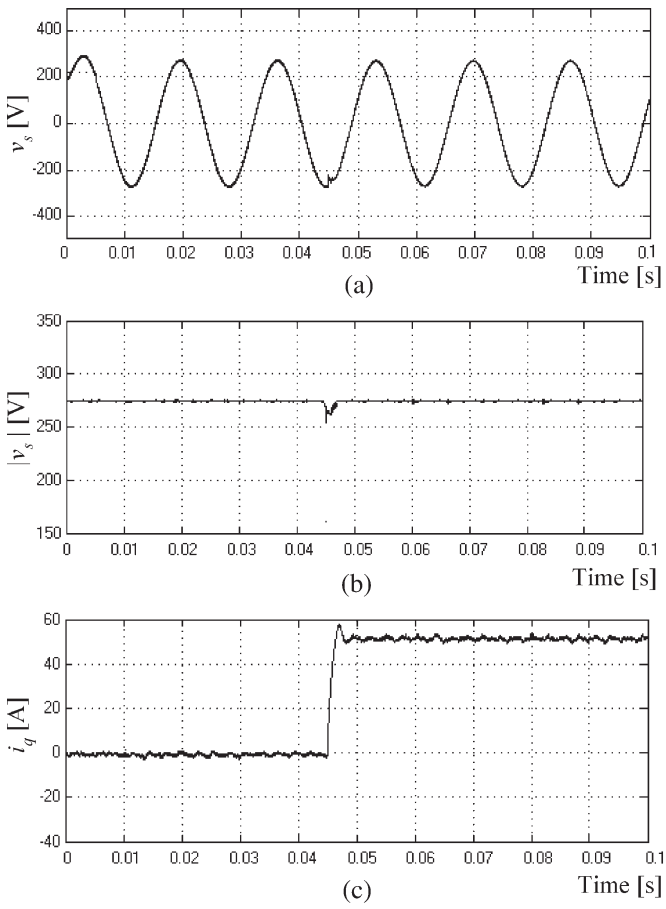

Fig. 9. Voltage regulation performance with the proposed controller at sudden loading of load L2. (a) Voltage waveform. (b) Voltage magnitude at the PCC. (c) Reactive current injected.

Fig. 12 shows the grid voltage at the PCC during unbalanced voltage disturbance initiated by heavily unbalanced loading to emulate unsymmetrical fault conditions.

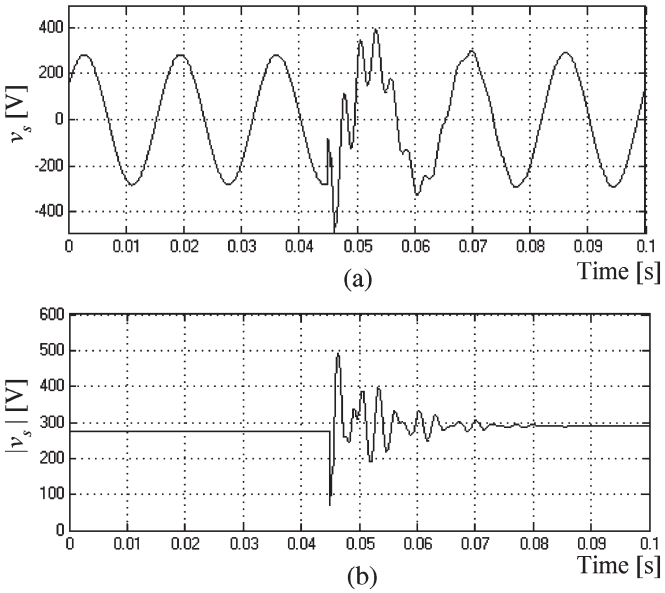

Fig. 10. Voltage transients due to capacitor switching. (a) Voltage waveform. (b) Voltage magnitude at the PCC.

A relatively large unbalanced voltage dip with 8.7% voltage unbalance factor [33] takes place for 9.6 cycles, by means of unbalanced loading, as shown in Fig. 12(a). The presence of the negative-sequence component leads to double power-frequency oscillations in the dq components of the grid voltage, as shown in Fig. 12(b).

Fig. 13 depicts the control performance of the proposed scheme under the unbalanced grid voltage illustrated in Fig. 12. Fig. 13(a) shows the three-phase voltages, which are well regulated under the unbalanced disturbance. Fig. 13(b) shows the positive-sequence dq components of the grid voltage, whereas Fig. 13(c) shows the corresponding negative-sequence components. Since the inverter interface is supporting the grid reactively in a fast manner, only the d-component of the positive-sequence grid voltage appears, whereas other sequence components swiftly vanish. Fig. 13(d) and (e) shows the sequence components of the injected current. The fast action of the proposed controller in regulating the line voltage is obvious. Provided that there is enough reactive power rating, the proposed interface can override larger voltage disturbances initiated by upstream grid faults.

The control chattering phenomenon associated with the VSC might counteract the stability and power quality requirements of the converter system. However, the switching function approximation can relax this problem. Fig. 14(a) shows the q-axis reference current command in the proposed controller with a hard switching function. The converter is commanded to start at $t = 0.045$ s under 12% reduction in the grid voltage magnitude. It is clear that the VSC voltage controller provides a good transient response to regulate the PCC voltage; however, the control chattering at the steady state is obvious. Fig. 14(b) shows the q-axis reference current command with switching-function approximation. The transient response is almost preserved, whereas the steady-state performance is remarkably improved. A smooth reactive current reference with negligible ripples is obtained.

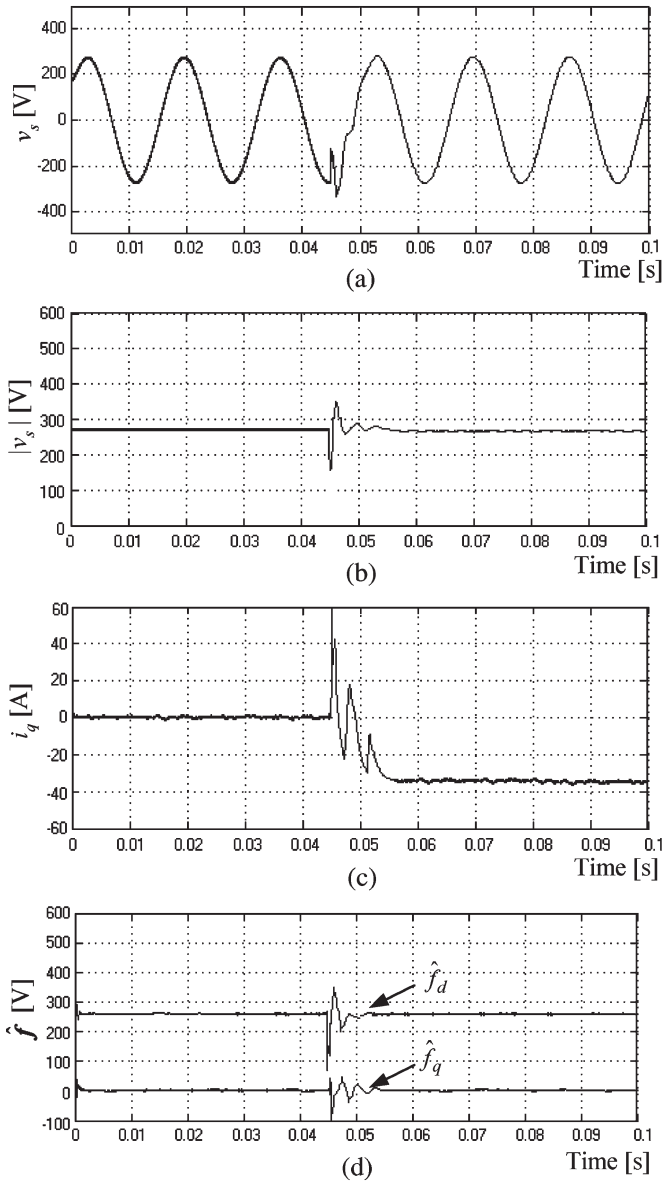

Fig. 11. Disturbance rejection performance with the proposed controller against voltage transients initiated by capacitor switching. (a) Voltage waveform. (b) Voltage magnitude at the PCC. (c) Reactive current injected. (d) Estimated uncertainty function.

V. Conclusion

In this paper, a control scheme for grid-connected PWM VSIs featuring fast load-voltage regulation and effective mitigation of fast voltage disturbances has been presented. A hybrid voltage controller combining a linear with VSC element has been proposed and applied to an inverter-based DG interface to regulate the voltage at the PCC. The proposed voltage controller successfully embeds a wide band of frequency modes through an equivalent internal model. Subsequently, a wide range of voltage perturbations, including capacitor-switching disturbances, has been effectively mitigated. To provide effective mitigation of unbalanced voltage disturbances, a dual-sequence voltage controller has been developed. Accordingly, the proposed interface can override unbalanced voltage disturbances initiated by upstream grid faults. To ensure accurate and robust tracking of the generated active and reactive current trajectories, a newly designed deadbeat current control algorithm has been presented. The current controller has been designed under the practical considerations of inherent plant delays, associated with the digital implementation of the control algorithm, and the uncertain nature of the current dynamics. Theoretical analysis and comparative evaluation tests are presented to demonstrate the effectiveness of the proposed control scheme.

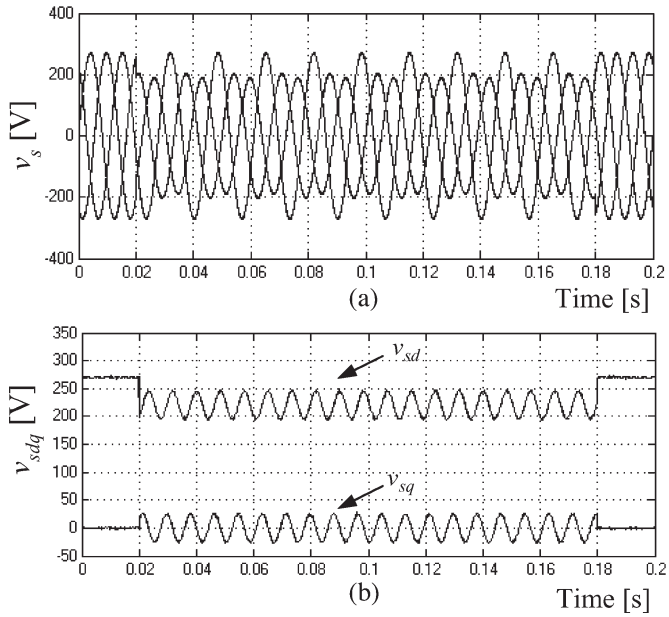

Fig. 12. Grid voltage at the PCC during unbalanced voltage disturbance. (a) Voltage waveforms. (b) Grid voltage dq components.

Appendix A

To derive the adaptation law in (31), a Lyapunov function candidate is selected as

$$V\Big(\boldsymbol{e}(t),\widetilde{\boldsymbol{d}}(t),t\Big)=\boldsymbol{e}^T\boldsymbol{P}\boldsymbol{e}+\frac{1}{\eta}\widetilde{\boldsymbol{f}}^T\widetilde{\boldsymbol{f}}. \tag{33}$$

The time derivative of (33) is derived as

$$\begin{aligned}V\Big(\boldsymbol{e}(t),\widetilde{\boldsymbol{f}}(t),t\Big)&=\boldsymbol{e}^T(\boldsymbol{A}_{\boldsymbol{co}}^T\boldsymbol{P}+\boldsymbol{P}\boldsymbol{A}_{\boldsymbol{co}})\boldsymbol{e}+2\widetilde{\boldsymbol{f}}^T\boldsymbol{G}_{\boldsymbol{co}}^T\boldsymbol{P}\boldsymbol{e}\\&\quad+\frac{2}{\eta}\widetilde{\boldsymbol{f}}^T\dot{\widetilde{\boldsymbol{f}}}\\&=-\boldsymbol{e}^T\boldsymbol{Q}\boldsymbol{e}+2\widetilde{\boldsymbol{f}}^T\boldsymbol{G}_{\boldsymbol{co}}^T\boldsymbol{P}\boldsymbol{e}+\frac{2}{\eta}\widetilde{\boldsymbol{f}}^T\dot{\widetilde{\boldsymbol{f}}}.\end{aligned} \tag{34}$$

Assuming that the observed disturbance is naturally continuous with a bandwidth that is much smaller than the observation period and by using (31), the following result can be deduced:

$$V\Big(\boldsymbol{e}(t),\widetilde{\boldsymbol{f}}(t),t\Big)\le 0. \tag{35}$$

Therefore, a robust current control performance can be yielded.

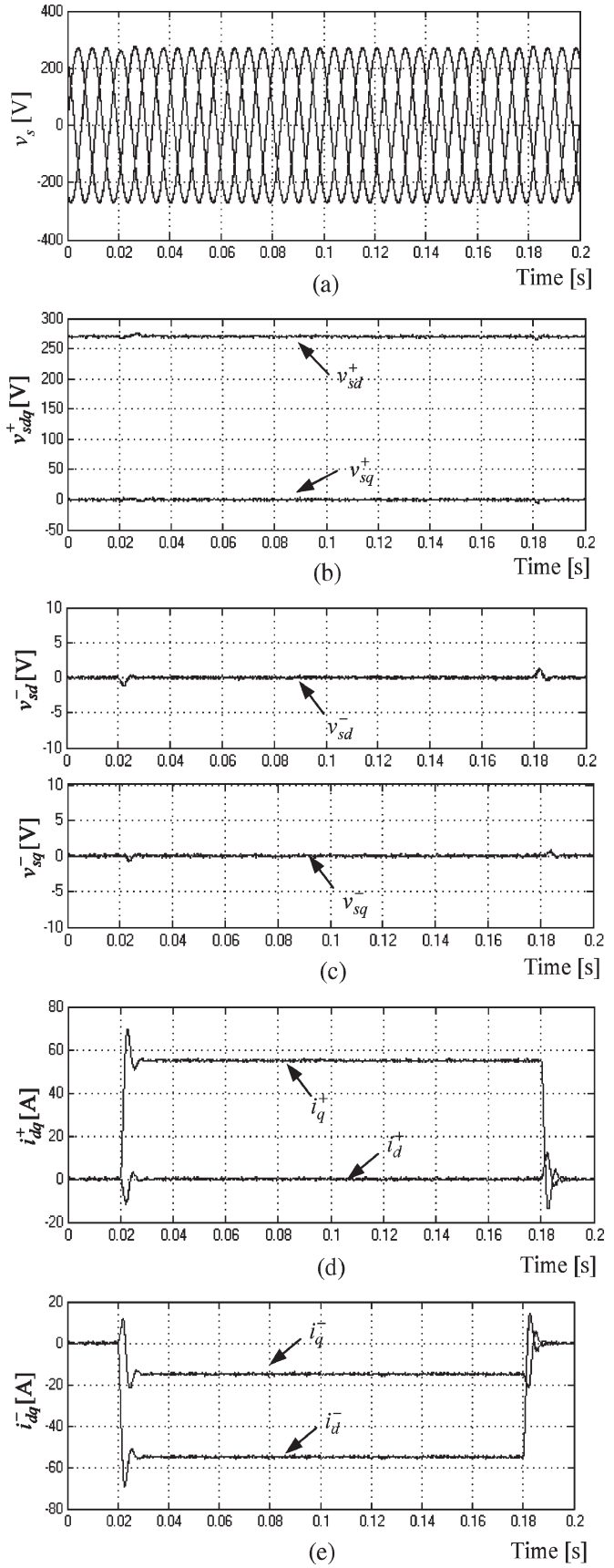

Fig. 13. Control performance of the proposed scheme during unbalanced voltage disturbance. (a) Voltage waveforms. (b) and (c) Positive- and negative-sequence dq components of the grid voltage. (d) and (e) Positive- and negative-sequence dq components of the injected currents.

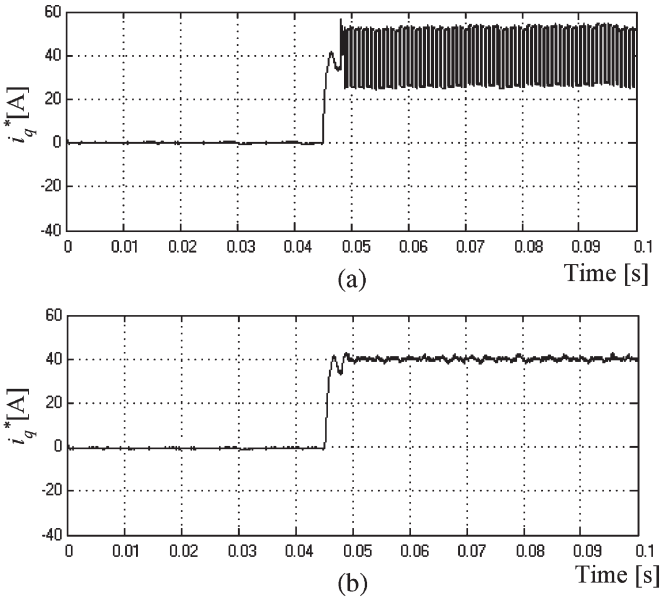

Fig. 14. Control effort of the proposed voltage controller (a) with a hard switching function and (b) with switching-function approximation.

APPENDIX B

The parameters of the studied system shown in Fig. 4 are given as follows:

- nominal grid phase-voltage at the PCC $= 110$ V at 60 Hz;
- $R_s = 0.08\ \Omega$;
- $L_s = 1$ mH;
- dc-link voltage $= 600$ V;
- load L1: 20 kW at a lagging power factor of 0.9;
- load L2: 30 kW at a lagging power factor of 0.85;
- switching capacitor: 20 kVAR;
- nominal equivalent interfacing inductance $L_o = 2.5$ mH;
- nominal equivalent interfacing resistance $R_o = 1.0\ \Omega$.

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REFERENCES

[1] A. Wolf and M. Thamodharan, "Reactive power reduction in three-phase electric arc furnace," *IEEE Trans. Ind. Electron.*, vol. 47, no. 4, pp. 729–733, Aug. 2000.

[2] C. Moreno, H. Duarte, and J. Garcia, "Propagation of flicker in electric power networks due to wind energy conversions systems," *IEEE Trans. Energy Convers.*, vol. 17, no. 2, pp. 267–272, Jun. 2002.

[3] A. Woyte, V. Thong, R. Belmans, and J. Nijs, "Voltage fluctuations on distribution level introduced by photovoltaic systems," *IEEE Trans. Energy Convers.*, vol. 21, no. 1, pp. 202–209, Mar. 2006.

[4] J. Gomez and M. Morcos, "Voltage sag effects on sensitive equipment due to starting cycles of induction motor," *IEEE Power Eng. Rev.*, vol. 22, no. 8, pp. 51–52, Aug. 2002.

[5] N. Kolcio, J. Halladay, G. Allen, and E. Fromholtz, "Transient overvoltages and overcurrents on 12.47 kV distribution lines: Field test results," *IEEE Trans. Power Del.*, vol. 7, no. 3, pp. 1359–1370, Jul. 1992.

[6] A. Jain, K. Joshi, A. Behal, and N. Mohan, "Voltage regulation with STATCOMs: Modeling, control and results," *IEEE Trans. Power Del.*, vol. 21, no. 2, pp. 726–735, Apr. 2006.
[7] P. W. Lehn and M. R. Iravani, "Experimental evaluation of STATCOM closed loop dynamics," *IEEE Trans. Power Del.*, vol. 13, no. 4, pp. 1378–1384, Oct. 1998.
[8] H. Fujita and H. Akagi, "Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1046–1053, May 2007.
[9] M. Marei, E. El-Saadany, and M. Salama, "A novel control algorithm for the DG interface to mitigate power quality problems," *IEEE Trans. Power Del.*, vol. 19, no. 3, pp. 1384–1392, Jul. 2004.
[10] M. Morari and E. Zafiriou, *Robust Process Control*. Englewood Cliffs, NJ: Prentice-Hall, 1989.
[11] G. Weiss, Q. Zhong, T. Green, and J. Liang, "H_∞ repetitive control of DC-AC converters in microgrids," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 219–230, Jan. 2004.
[12] Y. Yildiz, A. Sabanovic, and K. Abidi, "Sliding-mode neuro-controller for uncertain systems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 3, pp. 1676–1685, Jun. 2007.
[13] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: A survey," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 691–703, Oct. 1998.
[14] B. K. Bose, "An adaptive hysteresis-band current control technique of a voltage-fed PWM inverter for machine drive system," *IEEE Trans. Ind. Electron.*, vol. 37, no. 5, pp. 402–408, Oct. 1990.
[15] C. T. Pan and T. Y. Chang, "An improved hysteresis current controller for reducing switching frequency," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 97–104, Jan. 1994.
[16] D. N. Zmood, D. G. Holmes, and G. H. Bode, "Frequency-domain analysis of three-phase linear current regulators," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 601–610, Mar./Apr. 2001.
[17] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 814–822, May 2003.
[18] S. Fukuda and R. Imamura, "Application of a sinusoidal internal model to current control of three-phase utility-interface converters," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 420–426, Apr. 2005.
[19] T. M. Rowan and R. J. Kerkman, "A new synchronous current regulator and an analysis of current regulated PWM inverters," *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 4, pp. 678–690, Jul./Aug. 1986.
[20] C. T. Rim, N. S. Choi, G. C. Cho, and G. H. Cho, "A complete DC and AC analysis of three-phase controlled-current PWM rectifier using circuit D-Q transformation," *IEEE Trans. Power Electron.*, vol. 9, no. 4, pp. 390–396, Jul. 1994.
[21] T. G. Habetler, "A space vector-based rectifier regulator for AC/DC/AC converters," *IEEE Trans. Power Electron.*, vol. 8, no. 1, pp. 30–36, Jan. 1993.
[22] H. Le-Huy, K. Slimani, and P. Viarouge, "Analysis and implementation of a real-time predictive current controller for permanent-magnet synchronous servo drives," *IEEE Trans. Ind. Electron.*, vol. 41, no. 1, pp. 110–117, Feb. 1994.
[23] J. Mossoba and P. Lehn, "A controller architecture for high bandwidth active power filters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 317–325, Jan. 2003.
[24] H. Abu-Rub, J. Guzinski, Z. Krzeminski, and H. A. Toliyat, "Predictive current control of voltage-source inverters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 585–593, Jun. 2004.
[25] O. Kukrer, "Discrete-time current control of voltage-fed three-phase PWM inverters," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 260–269, Mar. 1996.
[26] H.-T. Moon, H.-S. Kim, and M.-J. Youn, "A discrete-time predictive current control for PMSM," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 464–472, Jan. 2003.
[27] G. H. Bode, P. C. Loh, M. J. Newman, and D. G. Holmes, "An improved robust predictive current regulation algorithm," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1720–1733, Nov./Dec. 2005.
[28] L. Springob and J. Holtz, "High-bandwidth current control for torque-ripple compensation in PM synchronous machines," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 713–721, Oct. 1998.
[29] Y. A.-R. I. Mohamed and E. F. El-Saadany, "An improved deadbeat current control scheme with a novel adaptive self-tuning load model for a three-phase PWM voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 747–759, Apr. 2007.
[30] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
[31] K. J. Astrom and B. Wittenmark, *Adaptive Control*. New York: Addison-Wesley, 1995.
[32] *IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems*, IEEE Standard 1547-2003.
[33] C.-Y. Lee, "Effects of unbalanced voltage on the operation performance of a three-phase induction motor," *IEEE Trans. Energy Convers.*, vol. 14, no. 2, pp. 202–208, Jun. 1999.

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