

# Optimal capacitor allocation in radial distribution systems for loss reduction: A two stage method

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## ABSTRACT

This paper presents an efficient approach for capacitor allocation in radial distribution systems that determine the optimal locations and sizes of capacitors with an objective of reduction of power loss and improving the voltage profile. A loss sensitivity technique is used to select the candidate locations for the capacitor placement. The size of the optimal capacitor at the compensated nodes is determined simultaneously by optimizing the loss saving equation with respect to the capacitor currents. The performance of the proposed method (PM) was investigated on several distribution systems and it was found that significant voltage profile improvement and loss saving can be achieved by optimal allocation of capacitors in the system. However this method is sensitive to the distribution network configuration. In a 28 node feeder the matrix of capacitor sizing becomes close to singular or badly scaled and results may be inaccurate. In 85 node feeder the same matrix becomes singular and no solution obtained. For the 28 node feeder a two stage technique is proposed: a reconfiguration of the feeder in the first stage followed by optimal capacitor allocation as a second stage. For the 85 node feeder a slight movement of the capacitor location was sufficient to reach optimal capacitor allocation. The proposed two stage technique is also applicable to the 85 node feeder for given optimum configuration of the tie switches. Simulations, using genetic algorithm are conducted for the two (28 and 85 nodes) systems allowing detection of loss reduction and voltage improvement due to capacitor placement.

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## 1. Introduction

Optimal allocation of shunt capacitors on radial distribution systems is essential for power flow control, improving system stability, power factor correction, voltage profile management, and losses minimization. The solution techniques for the capacitor allocation problem can be classified into four categories [1]: analytical, numerical programming [2], heuristic [3,4], and artificial intelligence-based (AI-Based). AI-Based methods include genetic algorithms [5,6], simulated annealing [7], expert systems [8], artificial neural networks, and fuzzy logic [9,10]. A survey of all capacitor allocation categories has been presented in [1,11]. Haque [12] proposed a method for minimizing the loss associated with the reactive component of branch currents by placing optimal capacitors at proper locations. The method first finds the location of the capacitors in a sequential manner (loss minimization by a singly located capacitor). The optimal capacitor size at each selected location for all capacitors are determined simultaneously, to avoid over compensation at any location, through optimizing the loss saving equation. Other publications found optimal capacitor size through

optimizing cost saving [13,14]. Capacitor locations are determined by two methods: Loss Sensitivity Factor and Index Vector. Capacitor sizes are determined by PSO. Capacitor locations given by two methods are not same and the sizes are also different in both the methods. But, total reactive power used for compensation is almost nearer to each other. Location of the capacitors may be found in sequential manner by loss minimization by a singly located capacitor [12,15]. Also fuzzy expert system may be used for extracting suitability of capacitor location from power loss reduction index and voltage profile [10]. Hsiao et al. [16] present a combination fuzzy-GA method to resolve the capacitor placement problem. The problem formulation considers three distinct objective functions related to minimize the total cost for energy loss and capacitors to be installed, as well as decreasing the deviation of bus voltage and improving the margin loading of feeders. Das [17] presents a genetic algorithm (GA) based fuzzy multi-objective approach for determining the optimum values of fixed and switched shunt capacitors to improve the voltage profile and maximize the net savings in a radial distribution system.

This paper, extending the problem formulation of previous researches on capacitor optimization presents an efficient approach for capacitor placement in radial distribution systems that determine the optimal locations and size of capacitor with an objective of reduction of power loss and improving the voltage

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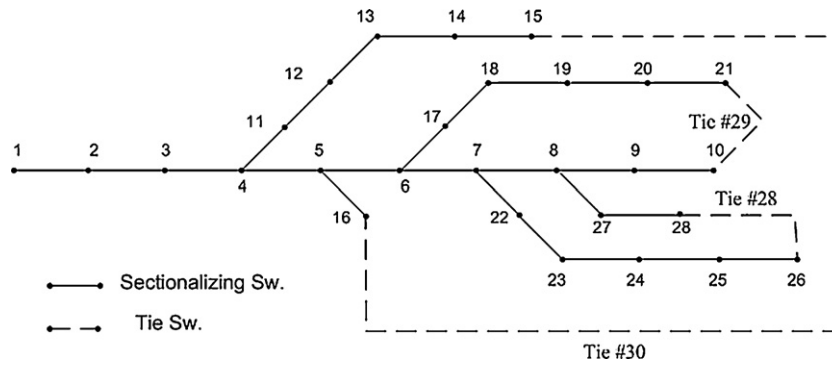


Fig. 1. Single line diagram of 28 node radial distribution feeder.

profile. A loss sensitivity technique is used to select the candidate locations. The size of the optimal capacitor at the compensated nodes is determined simultaneously by optimizing the loss saving equation with respect to the capacitor currents. Sensitivity measured through sequential loss minimization or suitability index extracted from fuzzy expert system gave same location of capacitors along distribution feeders. The performance of the PM was investigated on several distribution systems (15 node [18], 28 node [19], 33 node [15], 34 node [1], 69 node [3] and 85 node [18] feeders) and it was found that significant voltage profile improvement and loss saving can be achieved by optimal allocation of capacitors in the system. Two incidents were met where the configuration of distribution network may hinder the solution of capacitor allocation problem. In a 28 node feeder the matrix of capacitor sizing becomes close to singular or badly scaled and results may be

inaccurate. In 85 node feeder the same matrix becomes singular and no solution obtained. For the 28 node feeder a two stage capacitor allocation technique is applied: a reconfiguration of the feeder in the first stage [20] followed by optimal capacitor allocation as a second stage resulting in problem solution. For the 85 node feeder a slight movement of the capacitor location is proposed to avoid matrix singularity. The proposed two stage technique is also applicable to the 85 node feeder for given optimum allocation of the tie switches.

## 2. Proposed method

The load flow algorithm described in [21] is used for calculation of active and reactive power loss. Note that for a given configuration of a single-source radial network, the active power loss cannot

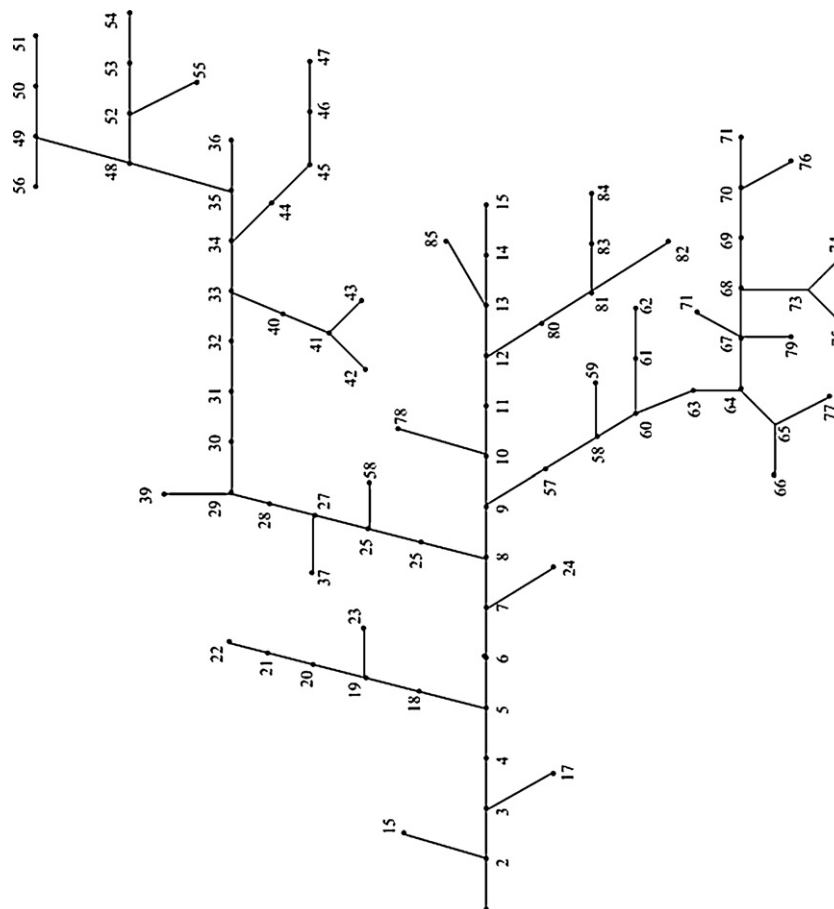


Fig. 2. Single line diagram of 85 node radial distribution feeder.

**Table 1**  
Summary of compensation by a multiple capacitors.

| System  | Power losses compensated/uncompensated (kW) | Capacitor location (node) and size (kVAr)                        | Power loss reduction (%) | Minimum voltage (pu) compensated/uncompensated | Money saving (\$) | CPU time (s) |
|---------|---|--|--------------------------|--|-------------------|--------------|
| 15 Node | 32.7697/61.7803                             | 3<br>6<br>925<br>375<br>Total = 1300                             | 46.96                    | 0.9725/0.9445                                  | 15567.31          | 2.593        |
|         | 32.4262/61.7803                             | 3<br>6<br>4<br>175<br>375<br>750<br>Total = 1300                 | 47.51                    | 0.9695/0.9445                                  | 15763.13          | 2.783        |
|         | 146.6393/210.7977                           | 7<br>29<br>850<br>875<br>Total = 1725                            | 30.44                    | 0.9245/0.9038                                  | 35284.88          | 2.868        |
|         | 144.0420/210.7977                           | 7<br>29<br>30<br>850<br>25<br>900<br>Total = 1775                | 31.67                    | 0.9251/0.9038                                  | 36728.07          | 2.945        |
| 34 Node | 363.8938/471.3114                           | 21<br>20<br>1050<br>775<br>Total = 1825                          | 22.79                    |  |                   |              |
|         | 363.5452/471.3114                           | 21<br>20<br>19<br>1125<br>625<br>75<br>Total = 1825              | 22.87                    | 0.8968/0.8822                                  | 60066.89          | 3.496        |
|         | 385.9952/471.3114                           | 21<br>20<br>19<br>6<br>600<br>1175<br>1375<br>25<br>Total = 3175 | 18.10                    | 0.9041/0.8822                                  | 46264.39          | 3.496        |
|         | 149.2920/224.6893                           | 19<br>62<br>225<br>1100<br>Total = 1325                          | 33.59                    | 0.9284/0.9092                                  | 42046.14          | 4.899        |
| 69 Node | 148.9139/224.6893                           | 19<br>62<br>63<br>225<br>900<br>225<br>Total = 1350              | 33.75                    | 0.9289/0.9092                                  | 42243.02          | 5.361        |

be minimized because all active power must be supplied by the source at the root node. However, the reactive power loss can be minimized by supplying part of the reactive power demands locally. The *PM* first identifies a sequence of nodes to be compensated. A loss sensitivity technique is used to select the candidate capacitor locations. Loss reduction index is found in sequential manner by loss minimization by a singly located capacitor. As cross check fuzzy expert system is used for extracting suitability of capacitor location from power loss reduction index and improving the voltage profile within voltage constraints. The optimal capacitor sizes at selected locations are determined simultaneously, to avoid over compensation at any location, through optimizing the loss saving equation. This involves the solution of a set of linear algebraic equations.

### 2.1. Capacitor sizing

The reactive power loss in the original  $n$ -branches system is given by

$$P_{Lr} = \sum_{i=1}^n I_{rt}^2 R_i \quad (1)$$

Let us consider the following:

$k$ , is the number of capacitor nodes

$\mathbf{I}_c$  is the  $k$ -dimensional vector consisting of capacitor currents

$\alpha_j$  is the upstream branches from the  $j$ th capacitor node to the source node ( $j=1,2,\dots,k$ )

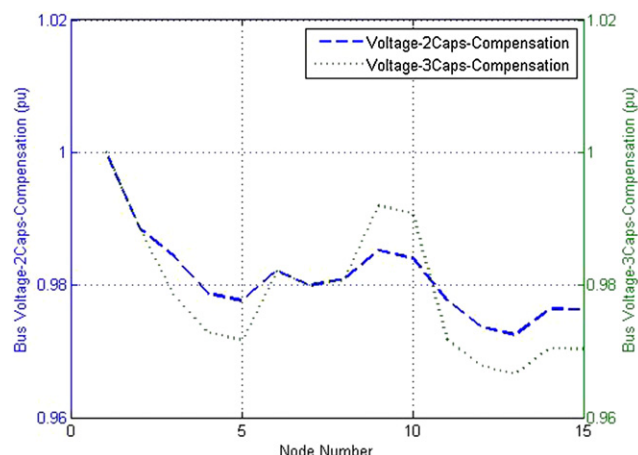
$\mathbf{D}$  is a matrix of dimension  $n$  by  $k$

The elements of  $\mathbf{D}$  are considered as:

$$D_i = 1; \text{ if branch } i \in \alpha$$
$$D_i = 0; \text{ otherwise}$$

When the capacitors are placed in the system, the new reactive component of branch currents are given by

$$[\mathbf{I}_r^{new}] = [\mathbf{I}_r] + [\mathbf{D}][\mathbf{I}_c] \quad (2)$$



**Fig. 3.** Voltage profiles on the compensated 15 node feeder with 2 and 3 capacitors.

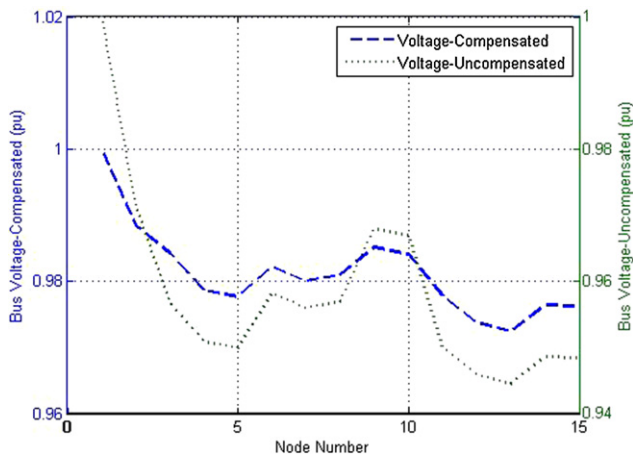


Fig. 4. Voltage profiles on the 15 node feeder before and after compensation.

Table 2

Optimal power-loss in each loop, tie-switch closed and sectionalize-switches open in the 28 bus reconfigured feeder.

| Tie switch (closed) | Sectionalize switches open between nodes | Power loss (kW) |
|---------------------|--|-----------------|
| 29                  | 9–10                                     | 68.3371         |
|                     | 8–9                                      | 68.0205         |
| 30                  | 5–6                                      | 67.8443         |
| 28                  | 25–26                                    | 64.5119         |
|                     | 24–25                                    | 63.9701         |
|                     | 23–24                                    | 64.1047         |

Last switching is not acceptable.

And the corresponding reactive power loss  $P_{Lr}^{comp}$  is

$$P_{Lr}^{comp} = \sum_{i=1}^n \left( I_{ri} + \sum_{j=1}^k D_{ij} I_{cj} \right)^2 R_i. \quad (3)$$

The loss saving  $S$  obtained by placing the capacitors is the difference between Eqs. (1) and (3) and is given by

$$S = - \sum_{i=1}^n \left[ 2I_{ri} \sum_{j=1}^k D_{ij} I_{cj} + \left( \sum_{j=1}^k D_{ij} I_{cj} \right)^2 \right] R_i \quad (4)$$

Table 3

Summary of compensation by a multiple capacitors for the 28 and 85 bus feeders.

| System                |            | Power losses compensated/uncompensated (kW) | Optimal capacitor locations (nodes) and sizes (kVAr) | Power loss reduction (%) | Minimum voltage (pu) compensated/uncompensated | CPU time (s) |
|-----------------------|------------|---|--|--------------------------|--|--------------|
| 228 Node              | Analytical | 29.9896/68.75858755                         | 6 225<br>7 475<br>Total = 700                        | 56.38 <sup>a</sup>       | 0.9633/0.9322 <sup>a</sup>                     | 4.0651       |
|                       | GA         | 35.4486/68.75858                            | 6 500<br>4 150<br>7 25<br>Total = 675                | 48.44 <sup>b</sup>       | 0.9532/0.9125 <sup>b</sup>                     | 34.9327      |
| 285 Node <sup>c</sup> | Analytical | 6185.2897/344.4759                          | 26 1200<br>9 1200<br>Total = 2400                    | 46.21                    | 0.9155/0.8707                                  | 5.9427       |

<sup>a</sup> Power loss reduction and voltage profile improvement due to feeder reconfiguration and optimal capacitor allocation

<sup>b</sup> Power loss reduction and voltage profile improvement due to optimal capacitor allocation using GA technique.

<sup>c</sup> Optimal capacitor allocation with shifting second capacitor from node #25 to node #26.

The optimal capacitor currents for the maximum loss saving can be obtained by solving the following equation:

$$\frac{\partial S}{\partial I_{c1}} = 0; \frac{\partial S}{\partial I_{c2}} = 0; \dots; \frac{\partial S}{\partial I_{ck}} = 0 \quad (5)$$

After some mathematical manipulations, Eq. (5) can be expressed by a set of linear algebraic equations as follows:

$$[A][I_c] = [B] \quad (6)$$

where  $A$  is a  $k$  by  $k$  square matrix and  $B$  is a  $k$ -dimensional vector. The elements of  $A$  and  $B$  are given by

$$A_{jj} = \sum_{i \in \alpha_j} R_i \quad (7)$$

$$A_{jm} = \sum_{i \in (\alpha_j \cap \alpha_m)} R_i \quad (8)$$

$$B_j = \sum_{i \in \alpha_j} I_{ri} R_i \quad (9)$$

The capacitor currents for the highest loss saving can be obtained from Eq. (6).

$$[I_c] = [A]^{-1}[B] \quad (10)$$

Once the capacitor currents are known, the optimal capacitor sizes can be written as

$$[Q_c] = [V_c][I_c] \quad (11)$$

Here  $V_c$  is the voltage magnitude vector of capacitor nodes. The saving in the compensated system can be estimated from Eq. (4) using the value of  $I_c$  given by Eq. (10). If the matrix of capacitor sizing, due to peculiar locations of capacitors becomes close to singular or badly scaled solution may be inaccurate. When the matrix is singular no solution will be obtained. A slight movement of the capacitor location will insure problem solution. However a two stage solution method is proposed as generic approach.

## 2.2. Two-stage optimal capacitor allocation

Capacitor locations in the 28 node feeder presented in Fig. 1 are at nodes 7 and 17. The upstream paths from these nodes are the same resulting in a close to singular or bad scaled  $[A^{-1}]$  or/and  $[B]$  matrices. In 85 node feeder presented in Fig. 2 the capacitor locations are at nodes 9 and 25. Also the upstream paths from these nodes are the same resulting in singular  $[A^{-1}]$  or/and  $[B]$  matrices and no solution obtained. For the 28 node feeder a two stage capacitor allocation technique is proposed: a reconfiguration of the feeder

**Table 4**  
Comparison of the proposed method results with previous publications.

| Items                              |  | Compensated/uncompensated |                              |               |                |                 |                              |                |               |                         |               |                       |               |
|------------------------------------|--|---------------------------|------------------------------|---------------|----------------|-----------------|------------------------------|----------------|---------------|-------------------------|---------------|-----------------------|---------------|
|                                    |  | [22] <sup>a</sup>         |                              |               |                |                 | [23] <sup>a</sup>            |                |               |                         |               | Proposed              |               |
| (a) 33-Bus System                  |  |                           |                              |               |                |                 |                              |                |               |                         |               |                       |               |
| Total losses (kW)                  |  | 135.4/202.67              |                              |               |                |                 | 135/203                      |                |               |                         |               | 144.04/210.80         |               |
| Optimal locations and sizes (kVAr) |  | 62829                     | 1200                         |               |                | 815202124262728 |                              |                |               |                         | 300           | 72930                 | 850           |
|                                    |  |                           | 760                          |               |                |                 |                              |                |               |                         |               |                       |               |
|                                    |  |                           | 200                          |               |                |                 |                              |                |               |                         |               |                       |               |
|                                    |  |                           |                              |               |                |                 |                              |                |               |                         |               |                       |               |
|                                    |  |                           |                              |               |                |                 |                              |                |               |                         |               |                       |               |
|                                    |  |                           |                              |               |                |                 |                              |                |               |                         |               |                       |               |
|                                    |  |                           |                              |               |                |                 |                              |                |               |                         |               |                       |               |
| Total kVAr                         |  | 2160                      |                              |               |                |                 | 2700                         |                |               |                         |               | 1755                  |               |
| Minimum voltage (pu)               |  | N/A                       |                              |               |                |                 | 0.9131/0.9349                |                |               |                         |               | 0.9251/0.9038         |               |
| CPU time (s)                       |  | N/A                       |                              |               |                |                 | N/A                          |                |               |                         |               | 2.944659              |               |
| Items                              |  | Compensated/uncompensated |                              |               |                |                 |                              |                |               |                         |               |                       |               |
|                                    |  | [24]                      | [25]                         | [26]          | [27]           | [28]            | [29]                         | [22]           | [30]          | [23]                    | [31]          | Proposed <sup>b</sup> |               |
| (b) 34-Bus System                  |  |                           |                              |               |                |                 |                              |                |               |                         |               |                       |               |
| Total losses (kW)                  |  | 168.47/221.67             | 168.95/221.72                | 168.95/221.72 | 169.14/221.72  | 161.33/221.72   | 167.91/221.72                | 168.50/221.67  | 168.80/221.72 | 170.00/221.67           | 168.98/221.67 | 163.47/221.67         |               |
| Optimal locations and sizes (kVAr) |  | 26, 11, 17, 4             | 19, 20, 21, 22, 23, 24, 25   | 18, 21, 19    | 18, 21, 19     | 8, 18, 25       | 20, 21, 22, 23, 24, 25, 26   | 19, 22, 20     | 19, 22, 20    | 5, 9, 12, 22, 26        | 24, 17, 7     | 8, 18, 25             |               |
|                                    |  | 1400, 750, 300, 250       | 683, 145, 144, 143, 143, 228 | 761, 803, 479 | 1200, 639, 200 | 1050, 750, 750  | 968, 145, 144, 143, 143, 228 | 1200, 739, 200 | 900, 986, 150 | 300, 300, 300, 600, 300 | 781, 803, 479 | 25, 2150, 875         |               |
| Total kVAr                         |  | 2700                      | 1629                         | 2063          | 2039           | 2550            | 2600                         | 2139           | 2036          | 1800                    | 2700          | 3050                  |               |
| Minimum voltage (pu)               |  | N/A                       | 0.9491/0.9417                | 0.9496/0.9417 | 0.9492/0.9417  | 0.9506/0.9417   |                              |                |               |                         |               | 0.9494/0.9417         |               |
| CPU time (s)                       |  |                           |                              |               |                |                 |                              |                |               |                         |               | 2.993898              |               |
| Items                              |  | Compensated/uncompensated |                              |               |                |                 |                              |                |               |                         |               |                       |               |
|                                    |  | [29]                      | [26]                         |               |                | [23]            |                              |                | [31]          | [32]                    | Proposed      |                       |               |
| (c) 69-Bus System                  |  |                           |                              |               |                |                 |                              |                |               |                         |               |                       |               |
| Total losses (kW)                  |  | 151.71/225.00             |                              |               | 152.48/224.98  |                 |                              | 147.40/224.98  |               | 156.62/224.96           |               | 152.72/225.02         | 148.91/224.79 |
| Optimal locations and sizes (kVAr) |  | 61<br>64                  | 1123                         |               | 46             | 781             |                              | 57             | 1200          | N/A                     |               | N/A                   | 225           |
|                                    |  |                           | 207                          |               | 47             | 803             |                              | 58             | 274           |                         |               | 62                    | 900           |
|                                    |  |                           |                              |               | 50             | 479             |                              | 61             | 200           |                         |               | 63                    | 225           |
| Total kVAr                         |  | 1330                      |                              |               | 2063           |                 |                              | 1674           |               |                         |               | 1350                  |               |
| Minimum voltage (pu)               |  | N/A                       |                              |               | N/A            |                 |                              | N/A            |               | 0.93693/0.90919         |               | 0.9289/0.9092         | 0.9289/0.9092 |
| CPU time (s)                       |  | N/A                       |                              |               | N/A            |                 |                              | N/A            |               | N/A                     |               | 4.471                 |               |

<sup>a</sup> Slight differences in load and line data.

<sup>b</sup> Same load and line data as in [20,23,24,25,26,27,21,28,20,29].

**Table 5**  
Improved results for the 34-Bus System.

| System  | Losses before compensation (kW) and min voltage (pu) | Capacitor location (node) | Capacitor size (kVAr)   | Losses after compensation (kW) and min voltage (pu) | Power loss reduction (%) | Money saving (k\$/yr) | CPU time (s) |
|---------|--|---------------------------|-------------------------|---|--------------------------|-----------------------|--------------|
| 34 Node | 221.6750.9417  | 9, 19 and 26              | 400 + 1000 + 800 = 2200 | 162.6360.9505                                       | 26.63                    | 32.013                | 3.256        |

in the first stage [20] followed by optimal capacitor allocation as a second stage. Simulation, using GA are applied to this feeder to detect power loss reduction achieved only from capacitor placement. For the 85 node feeder a slight movement of one capacitor location was sufficient to reach optimal capacitor allocation. The two stage technique is applicable also to the 85 node feeder.

### 3. Algorithm

The computational steps involved in finding the optimal capacitor size and location to minimize the loss in a radial distribution system are summarized in following:

1. Run the load flow program [21] and obtain the base case losses. Select a node and find the loss saving from Eq. (4) for the special case of singly located capacitor. Repeat this step for all Nodes in the system, except the source node. Identify the nodes that provides the highest loss saving.
2. Compensate two nodes to get the highest loss saving with the corresponding capacitors found from Eq. (11).
3. Repeat step 2 with three compensated nodes until it is found that no significant loss saving can be achieved by further capacitor placement.
4. If no solution is obtained due to the peculiar capacitor locations, apply the two stage solution method: feeder reconfiguration [20] then optimal capacitor allocation (steps 1–3). Perform simulation using genetic algorithm for the two (28 and 85 nodes) systems having peculiar capacitor locations. This allows detection of loss reduction and voltage improvement solely due to capacitor placement.

### 4. Simulation results

The PM of loss reduction by capacitor placement was tested on several distribution systems and results are given in Table 1. The table presents the corresponding \$-saving besides voltage improvement and CPU time requirements. Maximum power loss reduction was achieved, with two nodes compensated simultaneously for all investigated feeders. A third capacitor produces slight increase in loss reduction and money saving. However the voltage profile is not as good as with two capacitors in some cases as presented in Fig. 3 for the 15 node feeder. Better voltage profile can be achieved by placing more capacitors in other cases as for the 34 node feeder however this is associated power loss rise. Colored areas in the table are the final optimum solution taking into consideration that extra third/fourth capacitor increases maintenance burden. The shunt capacitors also improve the voltage profile and due to the higher voltage the active component of branch current  $I_a$  and hence active power loss for the constant power load model, is also reduced slightly. The voltage profiles along the feeders with multiple capacitor allocation are considerably improved as presented in Fig. 4 for the 15 node feeder. Capacitor locations in 28 node feeder are at nodes 7 and 17. The upstream paths from these nodes are the same resulting in close to singular  $[A]^{-1}$  matrix and the solution of Eq. (10) may be inaccurate. In 85 node feeder the capacitor locations are at nodes 9 and 25. The upstream paths from these nodes are the same resulting in singular  $[A]^{-1}$  matrix and no solution obtained. For the 28 node feeder the two stage

capacitor allocation technique: a reconfiguration of the feeder in the first stage [20] followed by optimal capacitor allocation as a second stage, is applied. Table 2 presents optimal power-loss in each loop, tie-switch closed and sectionalize-switches open as a result of feeder reconfiguration. Simulations, using GA are conducted for this feeder to detect of loss reduction and voltage improvement solely due to capacitor placement. For the 85 node feeder a slight movement of the second capacitor location from node #25 to node #26 was sufficient to reach optimal capacitor allocation. The corresponding results of optimal capacitor allocation for these two feeders are presented in Table 3. The two stage technique is also applicable to the 85 node feeder. It awaits optimum allocation of tie switches. Comparisons of the results of PM as applied on the 33-Bus System with those in [22,23], on the 34-Bus System with those in [9,22–30] and on the 69-Bus System with those in [23,26,29,31,32] are detailed in Table 4a–c, respectively. Better or closed results are obtained. Multitude of simulations conducted allows author to declare the following main points affecting optimal capacitor allocation are:

Selection the candidate locations of capacitor: Loss Sensitivity Factor and Index Vector and also fuzzy expert system has been used for extracting suitability of capacitor location from power loss reduction index and voltage profile. Capacitor locations given by three methods are not same and the sizes are also different in the methods.

Bounds of capacitor size selection: Relatively high capacitor steps within declared bound allow higher power loss reduction and better improvement in voltage profiles. Suitable bound of capacitor size, satisfying the constraint limit and also giving best possible result could only be found out by trial and error, which is extremely difficult task.

The 34-Bus System has been subjected to further investigations to satisfy Reviewer's comments. Results in the manuscripts were obtained allowing 25:25:3000 kVAr capacitors for the program to choose from. Now a test is conducted allowing 300:100:3000 kVAr capacitors for the program to choose from. Higher loss reduction and better voltage profile are obtained and detailed in Table 5.

### 5. Conclusions

A simple method of minimizing the loss associated with the reactive component of branch currents by placing capacitors in a radial distribution system has been proposed. The method first finds a sequence of nodes to be compensated through finding the highest loss saving by a singly located capacitor. The optimal size of multiple capacitors is then determined simultaneously by minimizing the loss saving equation with respect to the capacitor currents. A two stage optimal capacitor allocation is proposed when the capacitor locations hinder the problem solution. A reconfiguration of the feeder in the first stage followed by optimal capacitor allocation as a second stage resulted in problem solution. Simulations, using GA are conducted allowing detection of loss reduction and voltage improvement solely due to capacitor placement. Examples on several distribution networks show the robustness which indicates the method as an appealing alternative to utilities interested in planning radial distribution networks.



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