# A Low-Power, Linearized, Ultra-Wideband LNA Design Technique

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***Abstract*—This work proposes a practical linearization technique for high-frequency wideband applications using an active nonlinear resistor, and analyzes its performance with Volterra series. The linearization technique is applied to an ultra-wideband (UWB) cascode common gate Low Noise Amplifier (CG-LNA), and two additional reference designs are implemented to evaluate the linearization technique—a standard (without linearization) cascode CG-LNA and a single-transistor CG-LNA. The single-transistor CG-LNA achieves +6.5 to +9.5 dBm IIP3, 10 dB (max.) gain, and 2.9 dB (min.) NF over a 3–11 GHz bandwidth (BW); the LNA consumes 2.4 mW from a 1.3 V supply. The cascode linearized LNA achieves +11.7 to +14.1 dBm IIP3, 11.6 dB (max.) gain, and 3.6 dB (min.) NF over 1.5 to 8.1 GHz; the cascode LNA consumes 2.62 mW from a 1.3 V supply. Experimental results show that the linearization technique improves the cascode LNA's IIP3 by a factor of 3.5 to 9 dB over a 2.5–10 GHz frequency range.**

***Index Terms*—High frequency linearization, single-stage, ultra-wideband (UWB), low noise amplifier (LNA), common gate (CG), low power, RF.**

## I. Introduction

GROWING research on reconfigurable multi-band/multi-standard and ultra-wideband (UWB) transceivers has sparked increased interest in broadband LNA design. A broadband LNA must provide good input matching, high linearity, and low noise figure (NF) over a multi-GHz bandwidth (BW), while consuming little power and die area. To implement broadband impedance matching, a bandpass-filter-(BPF-) based, inductively degenerated common-source (CS) CMOS LNA and a SiGe common-emitter LNA have been proposed in [1] and [2], respectively. The BPF-based UWB CG-LNA first proposed in [3] reduces power and improves the linearity compared to the UWB CS-LNA. However, the large number of inductors requires large area and increases the NF [1]–[3]. Using a CG transistor for input matching is reported in [4]–[7], but the additional CS stage consumes more power and degrades the linearity. A differential UWB CG-LNA employs capacitive cross-coupling to reduce the NF [8], but this cross-coupling also increases the quality factor of the parallel RLC input network, reducing the matching BW.

A big design challenge for UWB LNAs is the stringent linearity requirement over a wide frequency range, due to the large numbers of in-band interferences in UWB system, and the cross-modulation/inter-modulation caused by blockers or transmitter leakage [6] in a reconfigurable receiver. Furthermore, while $f_T$ increases with technology scaling, linearity worsens due to lower supply voltage and high-field mobility effects [6]. Therefore, wideband linearization in deep-submicron CMOS process is a new trend. However, most of the linearization methods reported so far target applications that are either narrowband or have operating frequencies below 3 GHz [6], [9]–[17]. To the authors' knowledge, [7] is the first work to explore linearization technique for wideband LNAs with frequencies up to 6 GHz.

A linearization method for high-frequency wideband applications is desired. Optimizing the overdrive voltage $(V_{gs} - V_{th})$ [8], [10] leads to a linearity boost region for fairly narrow range of input amplitude, and an increased sensitivity to process variation. The feed-forward distortion cancellation technique [11]–[17] extends the linearity improvement region. In [11], a coaxial assembly is required for accurate power splitting which is not feasible for practical applications. The derivative superposition (DS) method [12]–[16] uses an additional transistor's nonlinearity to cancel that of the main device; it involves MOS transistors working in triode [12] or weak inversion region [13]–[15]; thus, these are mainly effective at relatively low frequencies. A bipolar in CMOS process is used [16] to push the operating frequency to 3 GHz. However, the common problem existing in all the reported DS methods is its difficulty to match the transistors working in different regions or match a bipolar with a MOS transistor, resulting in a linearity improvement highly sensitive to PVT variations, and sub-optimal nonlinearity cancellation in practice. The post-distortion method [17] uses all transistors in saturation region and also avoids the input matching degradation; however, the two cascode paths will introduce linearity and BW degradation at high frequencies [18], thus more inductors will be needed to avoid gain roll off for wideband application [3].

In this paper, a single-stage, low-power UWB CG-LNA is introduced, which has the simplest input matching network and the lowest power consumption compared to the prior reported single-ended UWB LNAs. Furthermore, a linearization technique is implemented on the single-stage cascode UWB CG-LNA. The added simple linearization circuitry does not affect the wideband input matching and has minimum power/area overhead.

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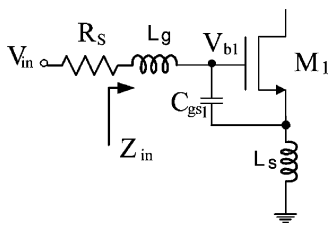


Fig. 1. Typical inductor-degenerated common source LNA.

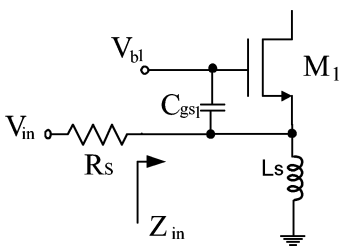


Fig. 2. Typical common gate LNA.

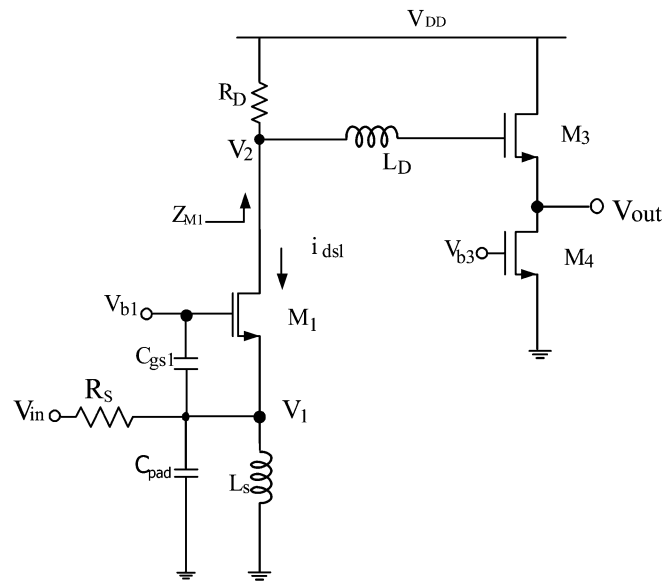


Fig. 3. Proposed single-stage single-transistor UWB CG-LNA.

TABLE I
CS-LNA VERSUS CG-LNA TOPOLOGIES

| Topology | $Z_{in}(s)$ seen from $R_s$ | $Q_{match}$ |
|---|---|---|
| CS-LNA | $\dfrac{s^2 + s\dfrac{g_{m1}L_s}{(L_s+L_g)C_{gs1}} + \dfrac{1}{(L_s+L_g)C_{gs1}}}{s/(L_s+L_g)}$ | $\dfrac{1}{2\omega C_{gs1}R_s}$ |
| CG-LNA | $\dfrac{s/C_{gs1}}{s^2 + s\dfrac{g_{m1}}{C_{gs1}} + \dfrac{1}{L_sC_{gs1}}}$ | $\dfrac{\omega C_{gs1}R_s}{2}$ |

Section II describes the properties of the typical CS-LNA and CG-LNA. Section III presents both the proposed single-stage, single-transistor UWB CG-LNA and the cascode (two-transistor) version, and analyzes their noise and linearity. Section IV presents the proposed linearization technique. Theory and simulation are compared, and the impact of PVT variations is discussed. Section V addresses the effects of the proposed linearization technique on the $S_{11}$ and NF of LNA. Measurement results and conclusions are presented in Section VI and Section VII, respectively.

## II. PROPERTIES OF THE CS-LNA AND CG-LNA

Figs. 1 and 2 show a typical inductively degenerated common-source LNA (CS-LNA) [19] and a common-gate LNA (CG-LNA), respectively. $C_{gs1}$ is the parasitic gate-to-source capacitance. Their input impedance $Z_{in}(s)$ seen by $R_s$ and the quality factor of the input matching network $Q_{match}$ are listed in Table I. For simplicity, all other parasitics and body effects are ignored.

A lower $Q_{match}$ results in a wider BW. Due to the relatively high Q of CS-LNAs' matching network, the CS-LNA cannot meet UWB matching requirements without advanced design techniques [1], [2], [21].

The CG-LNA, however, has a parallel resonant network with low $Q_{match}$. For example, $C_{gs1} = 0.3$ pF yields $Q_{match}(f = 5\text{ GHz}) = 0.24$ and hence $BW = 21$ GHz. Because $Q_{match}$ is proportional to $C_{gs1}$, $Q_{match}$ will decrease and thus BW will increase as technology scales. Therefore the CG-LNA can easily implement broadband impedance matching without many extra components, dramatically saving area and avoiding on-chip inductor resistive losses [3]–[8]. Besides the simple and robust input matching architecture, the CG-LNA also has better linearity, lower power consumption, and better input-output isolation [3].

The NF of the CS-LNA is generally superior to that of the CG-LNA, because the CG-LNA's NF is limited by $1/g_m$ input matching. However, the CG-LNA provides better noise performance for higher operating frequency ratios $\omega_0/\omega_T$, as its induced gate noise is only a weak function of $\omega_0/\omega_T$, while the CS-LNA's noise is proportional to $\omega_0/\omega_T$ [20].

## III. PROPOSED LOW POWER SINGLE-STAGE UWB CG-LNA

### A. Design Considerations of the Proposed CG-LNA

This paper details the design of two single-stage UWB CG-LNAs in 0.13 $\mu$m CMOS process—one single-transistor and the other two-transistors (cascode). The basic topologies are shown in Fig. 3 and Fig. 4. $C_{gs1}$ and $C_{pad}$ are the parasitic capacitance of transistor $M_1$ and the input pad respectively. $M_3$ and $M_4$ form a buffer to drive the test equipment and also emulate the input impedance of the mixer. $L_s$, $L_D$ and $L_c$ are on-chip spiral inductors. $L_s, C_{gs1}, C_{pad}$, and the equivalent impedance of $M_1$ form a parallel low-Q resonant network. Proper selection of the resonant frequency and Q matches the input to $R_s$ over the whole BW. Inductor $L_D$ is used to achieve flat gain [1]–[5], [8], [19].

The single-transistor LNA demonstrates the simplest topology for a UWB LNA. Adding transistor $M_2$ (Fig. 4) improves isolation and increases low frequency gain by about 2–3 dB; however, the parasitic capacitances of $M_2$ degrades gain, linearity, and NF at high frequency [18], [22]. Inserting inductor $L_c$ partially compensates this degradation [3].

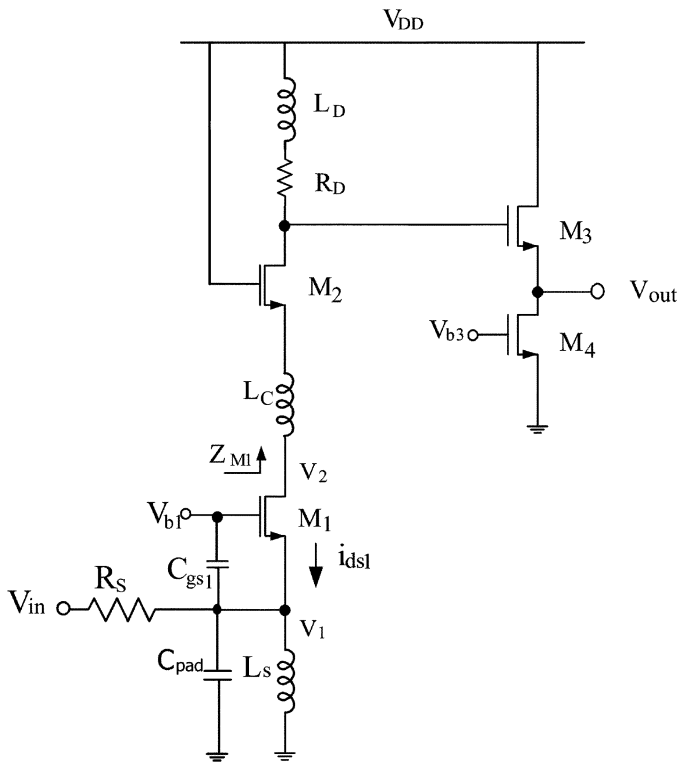


Fig. 4. Proposed single-stage cascode UWB CG-LNA.

### B. Noise Analysis of the Proposed CG-LNA

The overall transconductance of the CG-LNA in Figs. 3 and 4 is given by

$$G_m = \frac{i_{\mathrm{ds1}}}{V_{\mathrm{in}}} = \frac{|Z_{\mathrm{in}}(s)|}{|Z_{\mathrm{in}}(s) + R_s|} g_{m1} \tag{1}$$

where $Z_{\mathrm{in}}(s)$ is defined in Table I. The LNA noise factor is (neglecting $r_o$)

$$F = 1 + \frac{\gamma}{\alpha g_{m1} R_s} + \frac{\delta\alpha}{5 g_{m1} R_s}\left(\frac{\omega}{\omega_T}\right)^2 + \frac{R_D}{(\omega^2 L_D^2 + R_D^2)\, R_s g_{m1}^2 \left(\frac{Z_{\mathrm{in}}(s)}{Z_{\mathrm{in}}(s)+R_s}\right)^2} \tag{2}$$

where $\gamma, \alpha$, and $\delta$ are process-dependent parameters [19]. Because $L_c$ partially cancels the parasitic capacitance at the source node of cascode transistor $M_2$, its noise contribution remains much less than that of $M_1$ even at relatively high frequencies. The noise is dominated by the thermal noise (second term), which is mainly frequency-independent. The frequency-dependent gate induced noise (third term), and the frequency shaping of the resistor noise (fourth term) result in a small variation of the CG-LNA noise factor over the BW. The noise factor expression for CS-LNA and a detailed comparison for these two LNA topologies can be found in [20].

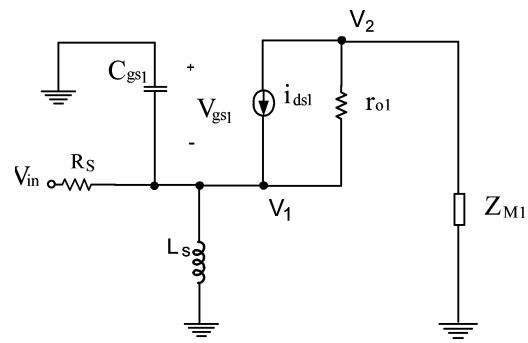


Fig. 5. Equivalent circuit of the CG-LNA input stage of Figs. 3 and 4.

### C. Linearity Analysis of the CG Input Stage

Fig. 5 shows the small-signal model for linearity analysis, where $Z_{M1}$ is the impedance looking out of the drain of $M_1$. The drain current of $M_1$ can be modelled up to third order as

$$i_{\mathrm{ds1}} = -g_{m1} v_1 + g_2 v_1^2 - g_3 v_1^3 \tag{3}$$

where $g_{m1}$, $g_2$ and $g_3$ are the main transconductance and the second/third order nonlinearity coefficients, respectively. Because capacitive and inductive (non-static) effects play an important role in LNA linearity, this work calculates the frequency-dependent harmonic-distortion coefficients using Volterra series. The relation between the source voltage $V_1$, the drain voltage $V_2$, and the input voltage $V_{\mathrm{in}}$ can be expressed up to third order as

$$V_1 = A_1(\omega) \mathrm{o} V_{\mathrm{in}} + A_2(\omega_1, \omega_2) \mathrm{o} V_{\mathrm{in}}^2 + A_3(\omega_1, \omega_2, \omega_3) \mathrm{o} V_{\mathrm{in}}^3 \tag{4}$$

$$V_2 = C_1(\omega) \mathrm{o} V_{\mathrm{in}} + C_2(\omega_1, \omega_2) \mathrm{o} V_{\mathrm{in}}^2 + C_3(\omega_1, \omega_2, \omega_3) \mathrm{o} V_{\mathrm{in}}^3 \tag{5}$$

where "o" is the Volterra series operator [23]. By solving KCL equations, we obtain expressions for the first and third order Volterra kernels:

$$A_1(\omega) = \frac{r_{o1} + Z_{M1}}{H(\omega)} \tag{6}$$

$$A_3(\omega_1, \omega_2, \omega_3) = \frac{A_1^3 \cdot R_s \cdot r_{o1} \cdot \varepsilon(\Delta\omega, \omega_1 + \omega_2)}{H(\omega_1 + \omega_2 + \omega_3)} \tag{7}$$

$$H(\omega) = R_s + r_{o1} + Z_{M1} + g_{m1} r_{o1} R_s + R_s B(\omega)(r_{o1} + Z_{M1}) \tag{8}$$

$$\varepsilon(\Delta\omega, \omega_1 + \omega_2) = g_3 - g_{\mathrm{o}B}(\Delta\omega, \omega_1 + \omega_2) \tag{9}$$

where $B(\omega) = j\omega C_{\mathrm{gs1}} + 1/j\omega L_s, g_{\mathrm{o}B}(\Delta\omega, \omega_1 + \omega_2) = (2)/(3) g_2^2 r_{o1} R_s [1/H(\Delta\omega) + 1/H(\omega_1 + \omega_2)], \Delta\omega = \omega_1 - \omega_2$, and $H(\omega)$ represents a transimpedance relating the input voltage to the nonlinear drain current. $\varepsilon(\Delta\omega, \omega_1 + \omega_2)$ shows how the second order ($g_{\mathrm{o}B}$) and third order ($g_3$) nonlinearity coefficients affect the third order distortion. The capacitive effect at the source of $M_1$ is resonated out by the inductor $L_s$, thus $B(\omega)$ remains small over the BW. Therefore, under the

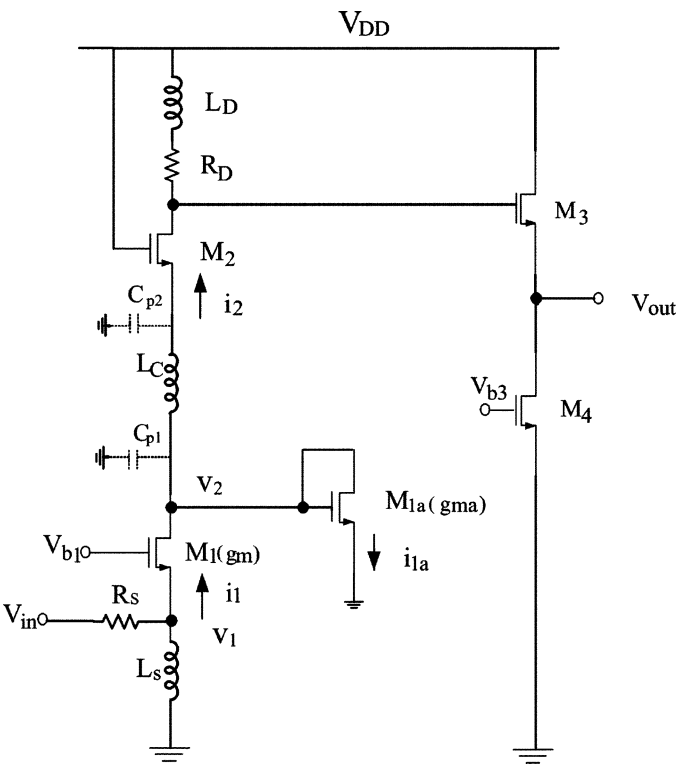


Fig. 6. Proposed linearized single-stage cascode UWB CG-LNA.

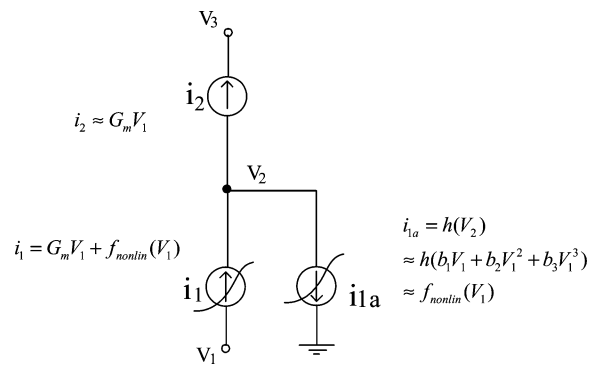


Fig. 7. Conceptual idea of the linearization technique.

input matching condition, $H(\omega)$ is simplified to a frequency-independent expression as

$$H(\omega) = R_s + 2r_{o1} + Z_{M1} \tag{10}$$

The Volterra kernel in (5) is calculated as

$$C_1(\omega) = -Z_{M1} \cdot A_1(\omega) \cdot \left(\frac{1}{R_s} + B(\omega)\right) + Z_{M1} \cdot \frac{1}{R_s} \tag{11}$$

$$C_3(\omega_1, \omega_2, \omega_3) = \frac{-Z_{M1} \cdot A_3(\omega_1, \omega_2, \omega_3) \cdot (1 + R_s B(\omega))}{R_s} \tag{12}$$

A linear $Z_{M1}$ results in a linear relation between $C_i(\omega)$ and $A_i(\omega)(i = 1, 3)$, and voltage $V_2$ is a linearly scaled version of $V_1$; however, if $Z_{M1}$ is nonlinear, then $V_2$ is a distorted version of $V_1$. The expression for IIP3 can be written as [7]

$$\mathrm{IIP3_{dBm}} = 20 \cdot \log_{10}\left(\sqrt{\left|\frac{4}{3}\frac{C_1(\omega)}{C_3(\omega_1, \omega_2, \omega_3)}\right|}\right) + 10\,\mathrm{dB}. \tag{13}$$

$C_1(\omega)$ is usually fixed by the design parameters, therefore low distortion is achieved by reducing $C_3(\omega_1, \omega_2, \omega_3)$ (i.e., by reducing $|\varepsilon(\Delta\omega, \omega_1 + \omega_2)|$). For a MOS transistor in saturation region, $g_3$ is negative and $g_{oB}$ is positive, so simultaneously reducing $g_3$ and $g_{oB}$ increases IIP3. The second order feedback paths that contribute to third order distortion in an LNA include the gate-drain capacitance $C_{gd}$ [13] and the source degeneration inductor $L_s$ [14], [15]. In the CG-LNA, the gate terminal of $M_1$ is AC grounded, reducing the feedback from $C_{gd}$. Thus, the third order distortion contributed by second order nonlinearity is smaller than in a CS-LNA. Section IV.C compares these theoretical calculations to simulation results.

Under matching condition, the input impedance $Z_{in}$ is estimated as $1/g_{m1}$, and (1) becomes

$$G_m = \frac{g_{m1}}{1 + g_{m1}R_s}. \tag{14}$$

Equation (14) is the same as for the resistive source degenerated transistor. Therefore, the linearity benefit of the resistive degeneration still holds true for the CG-LNA. From the above discussion, the CG-LNA has a better linearity than the CS-LNA.

## IV. Proposed High Frequency Linearization Technique

### A. Conceptual Idea of the Linearization Method

The cascode LNA has slightly worse linearity than a single-transistor LNA due to reduced headroom. Thus, the proposed linearization technique is implemented on the cascode LNA, as shown in Fig. 6. The inductor $L_c$ and the parasitic capacitances at the drain of $M_1$ and at the source of $M_2$ form a broadband $\pi$ network. Proper choice of $L_c$ cancels the capacitive effects, yielding effectively a short circuit over the whole BW. Under this condition, nonlinearity from $M_2$ can be neglected [18], leaving $M_1$ as the dominant source of nonlinearity. The diode connected transistor $M_{1a}$ linearizes $M_1$ as follows. First, model the drain currents of $M_1$ and $M_{1a}$ as

$$i_1 = g_m v_1 + g_2 v_1^2 + g_3 v_1^3 \tag{15}$$

$$i_{1a} = g_{ma} v_2 + g_{2a} v_2^2 + g_{3a} v_2^3. \tag{16}$$

Next, suppose $V_2$ is related to $V_1$ by

$$v_2 = b_1 v_1 + b_2 v_1^2 + b_3 v_1^3 \tag{17}$$

where $b_1$–$b_3$ are in general frequency dependent and can be extracted from simulation. In practice, the $\pi$ network cancels the effects of $b_2$ and $b_3$ at the frequency of interest [3]. The

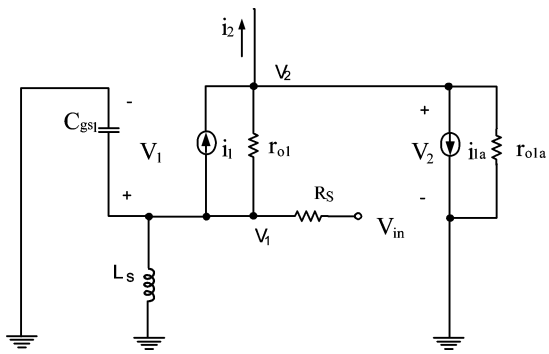


Fig. 8. Equivalent circuit for high frequency linearity analysis.

two nonlinear current $i_1$ and $i_{1a}$ add up at node $V_2$, yielding the output current $i_2$:

$$i_2 = i_1 - i_{1a} = (g_m - b_1 g_{\mathrm{ma}})v_1 + \left(g_2 - b_1^2 g_{2a} - b_2 g_{\mathrm{ma}}\right) v_1^2 + \left(g_3 - b_1^3 g_{3a} - g_{\mathrm{ma}} b_3 - 2 g_{2a} b_1 b_2\right) v_1^3. \quad (18)$$

To obtain a good IIP3, the third order distortion of the output current (third term in (18)) should be close to zero.

The LNA is initially designed to satisfy input matching, gain, NF, and power. Next, $M_{1a}$ is added to introduce additional degrees of freedom $g_{ma}$, $g_{2a}$, and $g_{3a}$ for linearity optimization. Fig. 7 illustrates the linearization technique. $M_{1a}$ taps voltage $V_2$ and replicates the nonlinear drain current of $M_1$, partially cancelling both second order and third order distortion terms. Though $M_{1a}$ partially cancels the linear term as well, it does not appreciably degrade the gain/NF because its bias is much less than that of $M_1$. Finally, note that $M_1$ and $M_{1a}$ uses identical finger sizes to improve matching and hence the cancellation of harmonics.

### B. High-Frequency Analysis With Volterra Series

Fig. 8 shows the CG-LNA schematic for high frequency distortion analysis. Since the parasitic capacitance associated with the drain of $M_1$ is absorbed by the LC $\pi$ network, it is not modelled here. The passive load resistance is much smaller than the transistor output resistance, thus we also neglect distortion due to nonlinear $r_o$. The analysis is limited up to third order, assuming a weakly nonlinear circuit. Solving KCL equations together with (4) and (15)–(17), the third order distortion of the output current ($i_{\mathrm{out,3rd}}$) can be calculated as

$$i_{\mathrm{out},3rd} = A_1(\omega)^3 \cdot \left[\left(g_3 - b_1^2 g_{3a}\right) - \frac{g_3'(g_m - b_1 g_{\mathrm{ma}})}{H(\omega)} + \frac{g_{\mathrm{oB}}'(\Delta\omega, \omega_1+\omega_2)(g_m - b_1 g_{\mathrm{ma}})}{H(\omega)} - \frac{\frac{2}{3}\left(g_2^2 - b_1^4 g_{2a}^2\right)}{H(\omega_1+\omega_2)}\right] \cdot v_{\mathrm{in}}^3 \quad (19)$$

$$A_1(\omega) = \frac{1}{R_s} \cdot \frac{1 + r_{o1}/r_{o1a}}{H(\omega)} \quad (20)$$

$$H(\omega) = \left(\frac{1}{R_s} + B(\omega)\right)\left(1 + \frac{r_{o1}}{r_{o1a}}\right) + \frac{1}{r_{o1a}} + \frac{r_{o1}}{r_{o1a}} g_m + b_1 g_{\mathrm{ma}} \quad (21)$$

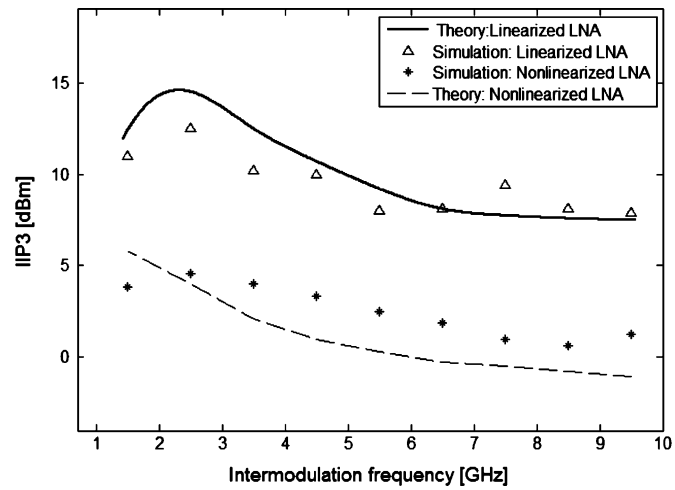


Fig. 9. IIP3 comparison of analytical expressions (13) and (19) with SPICE simulations for cascode LNA with and without linearization, using 100 MHz spacing two-tone with −20 dBm power level.

where

$$g_3' = (r_{o1})/(r_{o1a}) g_3 + b_1^3 g_{3\mathrm{a}},$$
$$g_{oB}'(\Delta\omega, \omega_1+\omega_2) = (2/3)((r_{o1})/(r_{o1a}) g_2 + b_1^2 g_{2\mathrm{a}})^2 \cdot (1/H(\Delta\omega) + (1/H(\omega_1+\omega_2))],$$
$$B(\omega) = j\omega C_{\mathrm{gs1}} + 1/j\omega L_s, \omega_1$$

and $\omega_2$ is the frequency of the two test tones. Equation (19) can be solved to obtain optimal IIP3. At the operating frequency, $B(\omega) \approx 0$, so $H(\omega)$ is a weak function of frequency. If $\omega_1 + \omega_2$ falls in band, then $H(\omega_1 + \omega_2)$ is also only weakly frequency-dependent. If $\omega_1 + \omega_2$ is out of band, thanks to the low Q input matching network, the imaginary part in $H(\omega_1 + \omega_2)$ is much smaller than the real part, making the frequency dependent effect still very small. Thus all the four terms in the bracket of (19) are approximately constant with respect to frequency, hence increasing the bandwidth of this linearization technique. This is verified by the measurement results shown later.

### C. Comparison of Analytical Expressions and Simulations

Fig. 9 compares the IIP3 calculated with Volterra series to that computed in SPICE. Two −20 dBm test tones separated by 100 MHz were swept from 1–10 GHz and applied to the cascode CG-LNA. As shown in Fig. 9, the theory predicts IIP3 frequency dependence quite well, the maximum deviation over the 1–10 GHz band is less than 2 dB. The obtained Volterra Series formulas can also predict the IIP3 variation as a function of two-tone spacing, as will be presented in Section VI.

### D. Process and Temperature Variations

To investigate the temperature sensitivity of the proposed linearization technique, post-layout IIP2/IIP3 simulations were conducted at −40°C, 27°C, and 85°C. IIP2 tests fixed one tone at 2.4 GHz and the other tone at 5.4, 3.1, and 5.6 GHz. IIP3 tests used 30 MHz tone spacing. In all cases, $P_{\mathrm{in}} = -20$ dBm. The 3 GHz, 5 GHz, and 8 GHz in Table II mean the intermodulation frequency (IM2 or IM3). IIP3 and IIP2 improvement above 4.4 dB and 4.7 dB respectively are achieved across temperature.

TABLE II
LINEARITY IMPROVEMENT VERSUS TEMPERATURE (POST-LAYOUT SIMULATION WITH TWO INPUT TONES AT −20 dBm)

| | Temperature / Inter-modulation freq. | -40°C | 27°C | 85°C |
|---|---|---|---|---|
| IIP3 Improvement (dB) | 3GHz | 11.5 | 8.2 | 6.1 |
| | 5GHz | 8.2 | 7.8 | 6 |
| | 8GHz | 9.1 | 5.8 | 4.4 |
| IIP2 Improvement (dB) | 3GHz | 10.2 | 8.5 | 4.7 |
| | 5GHz | 14.7 | 13 | 10.6 |
| | 8GHz | 9.4 | 7 | 5.3 |

The main effect of temperature variations is on $g_m(T)$ and $g_{ma}(T)$, since both $M_1$ and $M_{1a}$ work in saturation region and have same unit finger size, good matching is guaranteed, hence robust distortion cancellation is maintained across temperature variation.

To check the effect of process variation, pre-layout simulation was performed with a ±20% variation in the size of $M_{1a}$. Consistent IIP3 and IIP2 improvement above 7 dB and 5 dB respectively is obtained over the BW. These results verify the effectiveness of the linearization technique in a wide frequency range across process and temperature variations.

## V. EFFECTS OF THE LINEARIZATION TECHNIQUE ON $S_{11}$, AND NOISE FIGURE

Because $g_{m,M1a} \ll g_{m,M2}$, the input impedance $Z_{in}(s)$ seen from $R_s$ of the CG-LNA is about the same with and without linearizing transistor $M_{1a}$ present. Thus, $M_{1a}$ does not significantly affect matching. This is confirmed in both the simulation and measurement.

The channel noise and gate-induced noise of $M_{1a}$ appearing at the LNA output is

$$\overline{i^2_{nd,M_{1a}}} = 4kT\frac{\gamma}{\alpha}g_{m1a} \tag{22}$$

$$\overline{i^2_{ng,M_{1a}}} = 4kT\frac{\delta\alpha\omega^2 C^2_{gs,1a}}{5}\cdot\frac{g_{m1a}}{(g_{m1a}+g_{m2})^2}. \tag{23}$$

The noise contribution from $M_{1a}$ is proportional to its transconductance(i.e., $g_{m1a}$), which is much smaller than $g_{m1}$. The noise factor of the proposed linearized cascode CG-LNA can be calculated as

$$\begin{aligned} F = 1 &+ \frac{\gamma}{\alpha g_{m1}R_s} + \frac{\delta\alpha}{5g_{m1}R_s}\left(\frac{\omega}{\omega_T}\right)^2 \\ &+ \frac{R_D}{(\omega^2 L_D^2 + R_D^2)\,R_s g_{m1}^2\left(\frac{Z_{in}(s)}{Z_{in}(s)+R_s}\right)^2} \\ &+ \frac{\gamma}{\alpha g_{m1}R_s}\cdot\frac{g_{m1a}}{g_{m1}} + \frac{\delta\alpha}{5g_{m1}R_s}\left(\frac{\omega}{\omega_T}\right)^2 \\ &\cdot\frac{g_{m1a}}{g_{m1}}\cdot\frac{g_{m1a}^2}{(g_{m1a}+g_{m2})^2}. \end{aligned} \tag{24}$$

In (24), the last two terms are the additional noise contribution from the linearization circuitry, while the first four terms are from the cascode CG-LNA without linearization, as shown in (2). The 5th term is the channel noise of $M_{1a}$, which is smaller than the channel noise of $M_1$ by a factor of $g_{m1a}/g_{m1}$ (0.07 in our design). The 6th term—$M_{1a}$ gate induced noise—is $(g_{m1a}/g_{m1})^3 = 3.4\,e-4$ times smaller than the gate noise in $M_1$. Thus the degradation in NF is small—less than 0.6 dB over the entire measured BW. Based on the above discussion, the proposed linearization technique does not appreciably affect the input matching and NF.

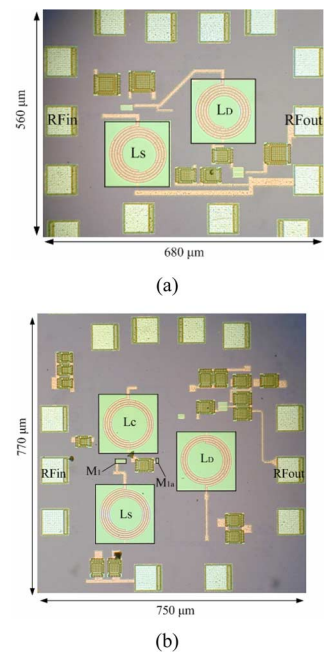


Fig. 10. Chip micrograph of (a) single-transistor UWB CG-LNA and (b) cascode UWB CG-LNA.

## VI. MEASUREMENT RESULTS

Both a single-transistor and a cascode single-stage UWB CG-LNA were fabricated in UMC 0.13 $\mu$m CMOS technology. The proposed linearization technique is implemented on the cascode LNA. The chip micrograph is shown in Fig. 10. The single-transistor CG-LNA core occupies 320 $\mu$m × 420 $\mu$m, and the cascode CG-LNA core uses 480 $\mu$m × 480 $\mu$m. The output buffer effect is de-embedded from the LNA+Buffer measurements using the measured results of a fabricated stand-alone buffer.

### A. Single-Transistor CG-LNA

Fig. 11 shows a maximum measured gain $S_{21} = 10$ dB with max variation ±1.5 dB over 3–11 GHz BW. $S_{11} < -10$ dB at high frequency (up to 12 GHz) but degrades slightly around 3 GHz. Fig. 12 indicates a minimum NF = 2.9 dB and variation <0.7 dB over 3–10 GHz.

In wideband operation, widely spaced tones will in practice dominate the IIP3 and IIP2. For example, the potential interferers for the UWB system include GPS, PCS/DCS, UMTS, ISM band (802.11 b/g, Bluetooth, Zigbee, IEEE 802.15.2, Microwave ovens), WiMax, and IEEE 802.11a. Thus the intermodulation products from the interferences with frequency spacing between tens of MHz to GHz need to be considered. For IIP2

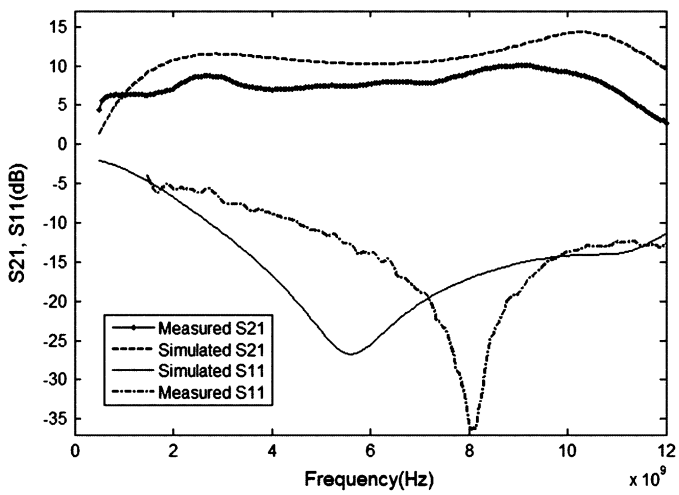


Fig. 11. S11 and S21 of the single-stage single-transistor CG-LNA (Fig. 3).

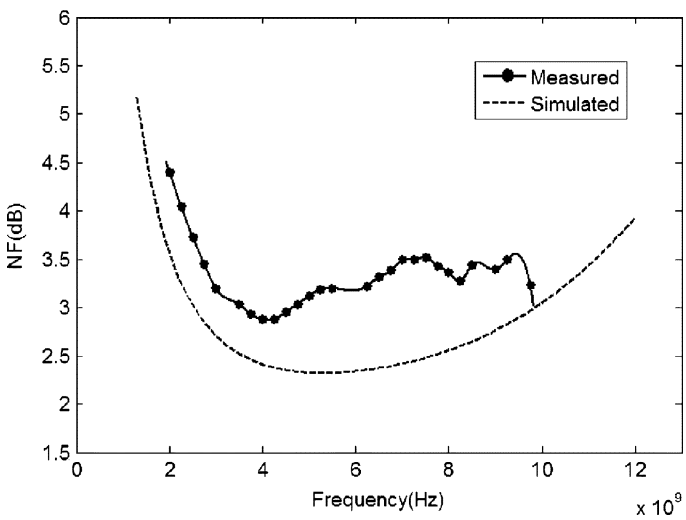


Fig. 12. Measured and simulated NF of the single-transistor CG-LNA.

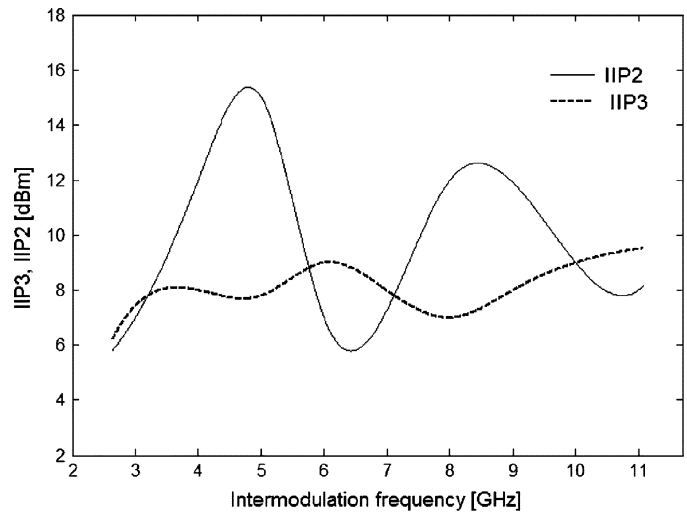


Fig. 13. Experimental IIP2, IIP3 for single-transistor LNA at different input frequencies.

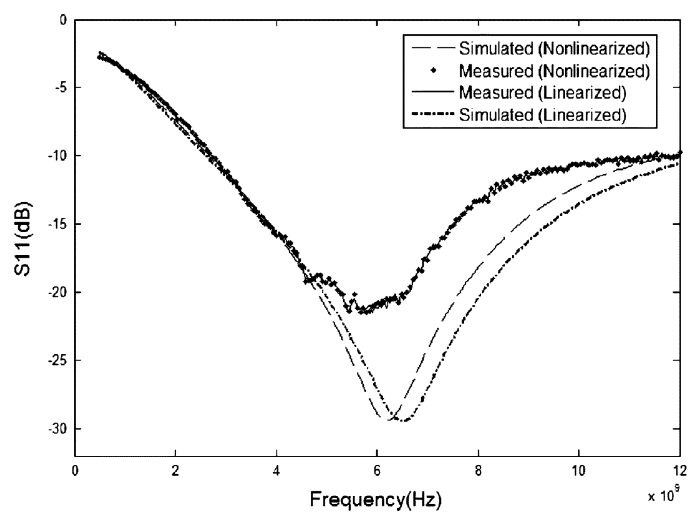


Fig. 14. Measured and simulated $S_{11}$ of the Cascode CG-LNA with (Fig. 6) and without linearization (Fig. 4).

measurement, one input tone is fixed at 5.2 GHz, while the other changes from 3 GHz to 9 GHz. For IIP3 measurement, we use two tones with 30 MHz spacing at: 2.8 GHz, 4.1 GHz, 5.1 GHz, 6.1 GHz, 7.1 GHz, 8.1 GHz, 9.1 GHz, 10.1 GHz, and 11.1 GHz. Fig. 13 shows the measured IIP2/3 performance of the single-transistor LNA. IIP2/3 were computed by $\mathrm{IIP2} = 2\mathrm{P_{in}} - \mathrm{P_{IM2}}$ and $\mathrm{IIP3} = \mathrm{P_{in}} + 0.5 * (\mathrm{P_{in}} - \mathrm{P_{IM3}})$, respectively, where $\mathrm{P_{in}}$ is the input power of one test tone in two-tone test, and $\mathrm{P_{IMk}}$ indicates the input referred power of the kth order intermodulation tone. In all cases, input tones have $\mathrm{P_{in}} = -20$ dBm. As shown in the figure, the single-transistor LNA achieves an IIP2 of 5–15 dBm and an IIP3 of 6.5–9.5 dBm. The measured IIP3 versus frequency spacing $(\Delta \mathrm{f_{in}})$ for the cascode LNA will be shown later. The UWB single-transistor LNA consumes only 1.85 mA from a 1.3 V power supply.

### B. Cascode CG-LNA

Fig. 14 shows an $\mathrm{S_{11}} < -10$ dB over the 2.7–12 GHz frequency range. As predicted by theory in Section V, the linearization method hardly affects $\mathrm{S_{11}}$. The discrepancy between simulation and test results is mainly attributed to the extra parasitic effects, and is significantly reduced when a 70 fF extra capacitance is added to the input node in simulation. As shown in Fig. 15, a 12.6 dB maximum gain with $\pm 1.5$ dB variation is obtained over the 0.8 GHz–8.4 GHz BW before linearization, the gain degradation remains below 1.7 dB over the entire band after linearization. As shown in Fig. 16, the LNA has a minimum NF as 3.3 dB, and a $\pm 0.75$ dB variation before linearization; the degradation in NF is less than 0.6 dB over the entire band after linearization. The variations in the NF arise from the frequency-dependent gate induced noise and the load resistor noise as shown in (2). The cascode transistor also contributes some frequency-dependant noise [18]. The UWB cascode LNA consumes only 2 mA from a 1.3 V power supply, and the linearization element only draws an additional 20 $\mu$A.

### C. Design Robustness

To experimentally verify the robustness of the linearization technique, the IIP3 and IIP2 of the cascode LNA with/without linearization were measured on ten randomly chosen chips.

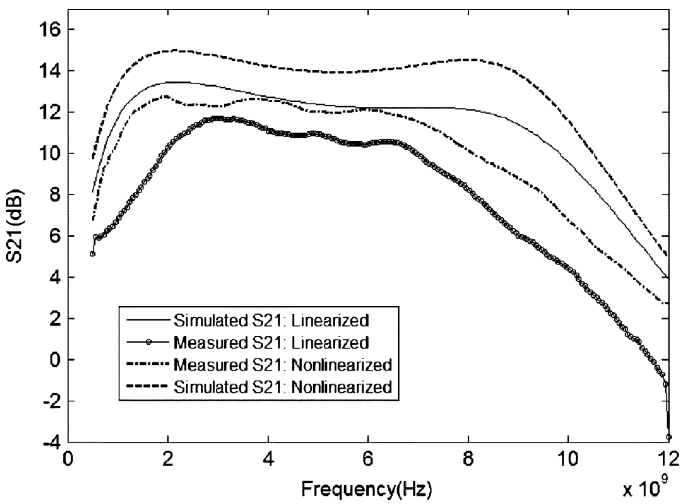


Fig. 15. Measured and simulated $S_{21}$ of the Cascode CG-LNA with (Fig. 6) and without linearization (Fig. 4).

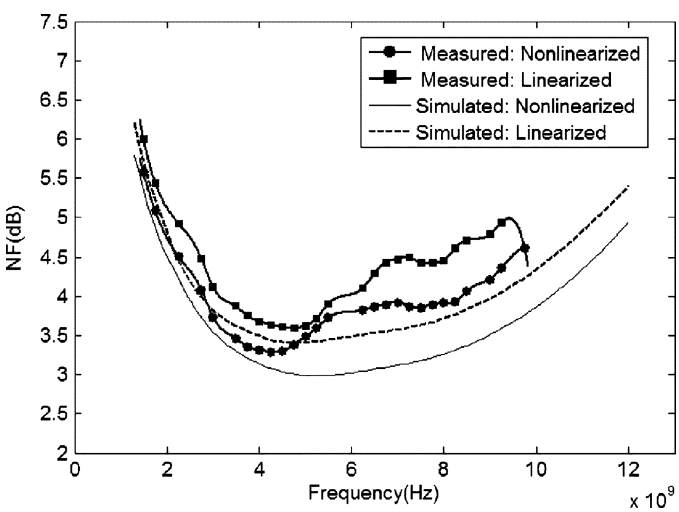


Fig. 16. Measured and simulated NF of the Cascode CG-LNA with (Fig. 6) and without linearization (Fig. 4).

The IIP3 of the cascode LNA was examined at seven different frequencies with 30 MHz frequency spacing at $-20$ dBm: 2.8 GHz, 4.1 GHz 5.1 GHz, 6.1 GHz, 8.1 GHz, 9.1 GHz, and 10.1 GHz. As shown in Fig. 17, an IIP3 improvement greater than 3.5 dB is achieved in worst case, while other samples showed an improvement as high as 9 dB. For IIP2 measurement, one input tone is fixed at 5.2 GHz, while the other changes from 3 GHz to 9 GHz, with equal power level as $-20$ dBm. Fig. 18 shows IIP2 improvement $>$3.3 dB in the worst case and improvement up to 10 dB in the best case. These results confirm the effectiveness and robustness of the proposed linearization technique over a wide frequency range. Because our technique utilizes all transistors in the saturation region, we obtain much better matching than previously reported methods that mixed and matched triode/weak-inversion transistors [12]–[15].

To check the sensitivity of IIP3 to two-tone spacing $(\Delta f_{in})$, IIP3 was also measured by fixing one input tone at 5 GHz while changing the other from 5.01 GHz to 7 GHz. Fig. 19 shows experimental and theoretical results (from (13) and (19)) of the

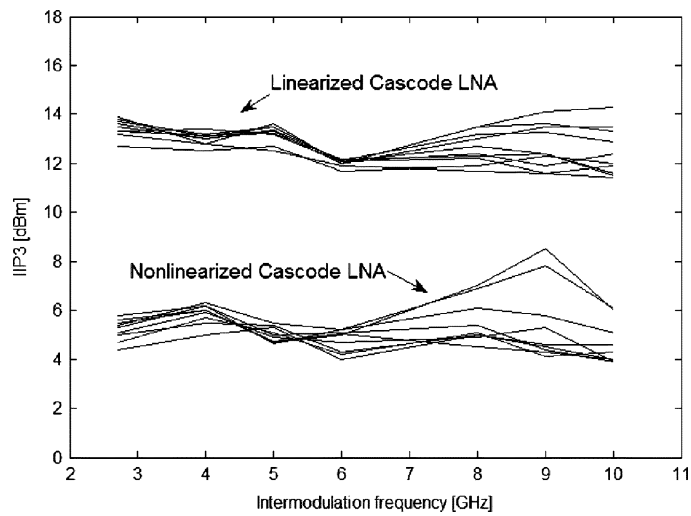


Fig. 17. Measured IIP3 (Cascode LNA) versus intermodulation frequency (10 samples).

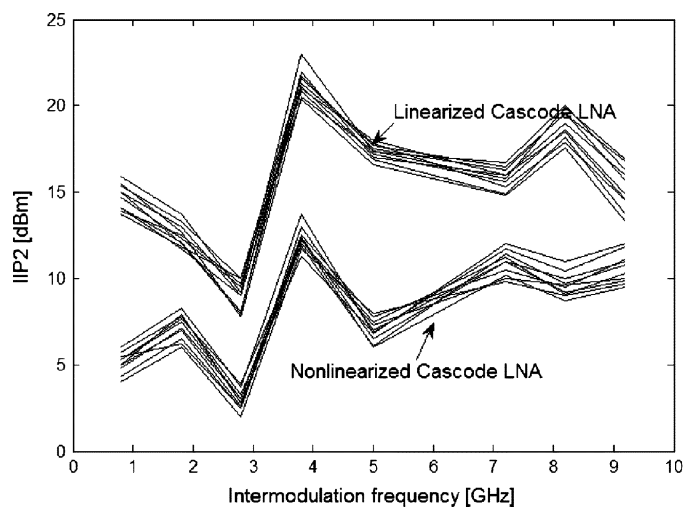


Fig. 18. Measured IIP2 (Cascode LNA) versus intermodulation frequency (10 samples).

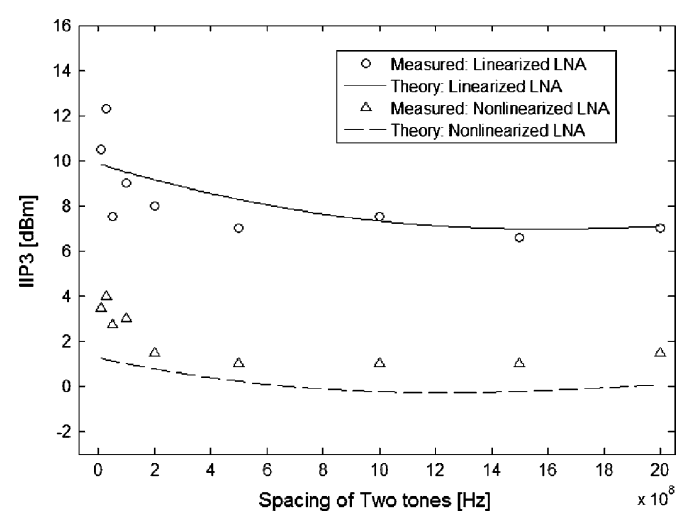


Fig. 19. Experimental and theoretical results of IIP3 for cascode LNA with and without linearization, as a function of frequency spacing for $-20$ dB input tones.

TABLE III
MEASUREMENT RESULTS SUMMARY AND CMOS UWB LNA COMPARISON

| Parameters | 3 dB BW [GHz] | S11 [dB] | S21 [dB] | NF [dB] | IIP3 [dBm] | IIP2 [dBm] | Power (core) [mW] | Area [mm$^2$] | FOM I | FOM II | CMOS Process |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ST CGLNA | 3~11 | <-7.5 | 7~10 | 2.9~3.6 | 6.5~9.5 | 5~15 | 2.4 | 0.38 | 22.3 | 149 | 0.13μm |
| Cascode CGLNA | 0.8~8.4 | <-9 | 9.6~12.6 | 3.3~5.5 | 3.9~8.5 [5)] | 1.8~13.9 [5)] | 2.6 | 0.58 | 21.8 | 109 | 0.13μm |
| Linearized CGLNA | 1.5~8.1 | <-9 | 8.6~11.7 | 3.6~6 | 11.7~14.1 [5)] | 7.6~23 [5)] | 2.62 | 0.58 | 12.9 | 261.6 | 0.13μm |
| [1]STD LNA | 2.3~9.2 | <-9.9 | 6.3~9.3 | 4~9 | -6.7 [2)] | -3~7 | 9 | 1.1 | 1.2 | 0.2 | 0.18μm |
| [1]TW LNA | 2.4~9.5 | <-9.4 | 7.4~10.4 | 4.2~9 | -8.8 [2)] | -10~0 | 9 | 1.1 | 1.5 | 0.2 | 0.18μm |
| [4] | 0.4~10 | <-10 | 9~12.4 | 4.4~6.5 | -6 [2)] | - | 12 | 0.42 | 3.9 | 0.97 | 0.18μm |
| [5] | 1.2~11.9 | <-11 | 6.7~9.7 | 4.5~5.1 | -4.9~-6.2 | 9.8~20 | 20 | 0.59 | 1.85 | 0.52 | 0.18μm |
| [7] | 0.2~5.2 | <-10 | 13~15.6 | 2.9~3.5 | 0~4 | 18~34 [5)] | 14 | 0.009 | 9.22 | 16.22 | 65nm |
| [8]LNA #1 [1)] | 1.3~10.7 | <-6 | 6.1~8.5 | 4.4~5.3 | 7.4~8.3 | - | 4.5 | 1.0 | 5.63 | 34.5 | 0.18μm |
| [8]LNA #2 [1)] | 1.3~12.3 | <-6 | 5.2~8.2 | 4.6~5.5 | 7.6~9.1 | - | 4.5 | 1.0 | 7.4 | 51.4 | 0.18μm |
| [25] | 3.1~10.6 | <-9.9 | 13.7~16.5 | 2.1~2.9 | -8.5~-5.1 | - | 9 | 0.87 | 35.97 | 8.1 | 0.13μm |
| [26] | 0.1~6.5 | <-10 | 17~19 | 3~4.2 | +1$^+$ | +4 [4)] | 12 | - | 26.37 | 33.23 | 0.13μm |
| [27] | 2~11 | <-8 | 9~12 | 5~6 | -4 [3)] | - | 16.8 | 0.7 | 2.1 | 0.9 | 90nm |
| [28] | 2~8 | - | 12 | 2.5 | +12 | - | 18 | - | 6.77 | 107.4 | 65nm |
| [29] | 0.6~10 | - | 10 | 3 | +6 | - | 30 [6)] | - | - | - | 45nm |

[1)] Differential LNA [2)] at 6GHz [3)] at 4GHz [4)] simulated [5)] for multiple samples
[6)] including VtoI converter
ST LNA: Single-Transistor LNA

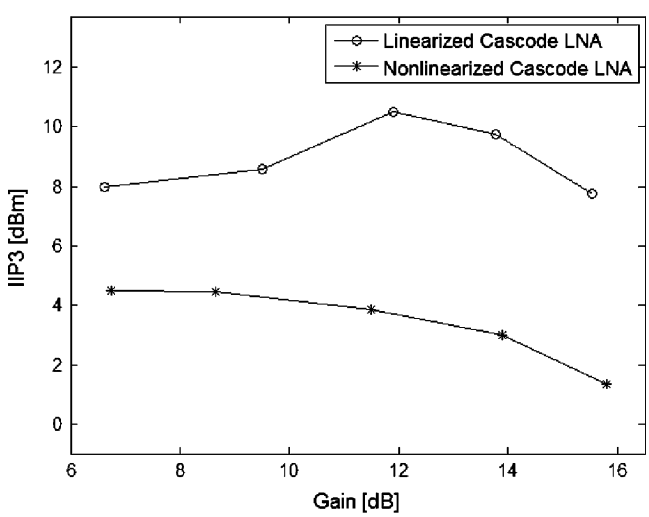


Fig. 20. Simulated IIP3 versus gain.

IIP3 as a function of $\Delta f_{in}$. IIP3 degrades by 4 dB when $\Delta f_{in}$ increases from 10 MHz to 200 MHz, and stays relatively constant with a variation less than 1 dB when $\Delta f_{in}$ increases up to 2 GHz. The Volterra series analysis in (7)–(13), (19)–(21) also indicates this trend. When $\Delta f_{in}$ is small, the parallel tank formed by $L_s$ and $C_{gs1}$ at the input has large susceptance (i.e., $B(\Delta\omega)$ is large), resulting in larger $H(\Delta\omega)$, smaller $g_{oB}$, and hence a smaller third order distortion coefficient. As $\Delta f_{in}$ increases, $B(\Delta\omega)$ decreases and remains small over the BW because of the low Q resonant network.

### D. Gain and Linearity

These two LNAs' gains are low because 1) they have only one stage; 2) their $g_m$s are limited by input matching; and 3) their output impedance is low(due to headroom limitations). The IIP3 is high not because of low gain since the primary source of nonlinearity is the drain current generated by the input transistor—hence a high impedance load will not degrade linearity provided that it is linear and does not disturb the transistor bias points. To prove this, a simulation is conducted: keeping the bias of input transistor constant, thus $g_m$, $g_{ds}$, and $I_{ds}$ is constant; change the load resistor $R_D$ and the power supply accordingly to keep the drain-to-source voltage of transistors constant. The inductor $L_D$ is also adjusted to maintain a flat gain over the BW. In this way we can vary the gain of the LNA to see its effect on IIP3. Two tones of 3.5 GHz and 3.65 GHz with $-20$ dBm power are used. Shown in Fig. 20, the IIP3 of the cascode LNA without linearization degrades 3.15 dB when gain varies from 6.8 dB to 15.8 dB; but an IIP3 improvement of 3.5–6.5 dB can be obtained over the whole gain variation range by applying the linearization technique. The small variation of 2 dB in IIP3 of the linearized cascode LNA with increasing gain proves that high IIP3 is not due to low gain.

The simulation result also proves that the proposed linearization technique is effective no matter what the LNA gain is. Thus as a general linearization technique, it can be applied to other LNA topologies, either with high gain or low gain. The only condition is, the linearization element must be added to a low

impedance node in order not to load the original LNA. This simulation also demonstrates that the LNA has the potential of obtaining larger gain thus better NF, while maintaining excellent linearity. This retains the advantage of low power consumption, at the cost of larger area and supply voltage. But in many applications the RF power amplifier and baseband analog signal processing circuits also run from a higher supply voltage than 1.2 V [6], [25], making this a viable alternative.

In the UWB "impulse radio" application, linear phase response across BW is also required to minimize phase distortion and recover the transmitted signal correctly. The S21 phase versus frequency for cascode LNA with and without linearization is simulated, and the maximum group delay variation is $<14\%$ over the entire BW. The linearization technique adds negligible group delay deviations.

Experimental results of the proposed LNAs and the prior published state-of-art UWB LNAs are summarized in Table III. For the comparison of different topologies, we include two figures of merit (FOMs) in the table—FOM_I [8], which does not include linearity, and FOM_II [24], which does:

$$\mathrm{FOM_}I = \frac{\mathrm{Gain_{average}}[abs] \times \mathrm{BW[GHz]}}{P_{\mathrm{dc}}[\mathrm{mW}] \times (F_{\mathrm{average}} - 1)} \tag{25}$$

$$\mathrm{FOM_}II = \frac{\mathrm{IIP3_{average}[mW]} \times \mathrm{Gain_{average}}[abs] \times \mathrm{BW[GHz]}}{P_{\mathrm{dc}}[\mathrm{mW}] \times (F_{\mathrm{average}} - 1)} \tag{26}$$

where $\mathrm{Gain_{average}}$ is the average gain, $\mathrm{F_{average}}$ is the average noise factor over the frequency range, and $\mathrm{P_{dc}}$ is the power consumption of the LNA core. From Table III, our proposed LNAs achieve comparable IIP3 with much less power than the previously reported best linearity in [8] and [28]. This is mainly due to the simple input matching network, single-stage architecture, and the proposed linearization technique. All three proposed LNAs exhibit comparable FOM_I, and much better FOM_II when compared to the other state-of-art UWB LNAs. The FOM_II of the linearized cascode LNA exhibits a factor of 2.4 over the best previously reported result in [28].

## VII. Conclusion

In this paper, a practical linearization technique is proposed for a UWB LNA, and a detailed linearity analysis using Volterra series is provided, which shows good agreement with simulation and experimental results. Three low-power single-stage UWB CG-LNAs are presented in this paper, with focus on the cascode LNA with linearization. The linearity of the proposed LNAs without linearization is also good because of the CG and single-stage topology. The UWB LNA was designed and fabricated in 0.13 $\mu$m UMC CMOS technology. Because all transistors operate in the saturation region, we obtain a robust linearity improvement over process and temperature variations. The proposed linearization method is experimentally demonstrated to improve the IIP3 by 3.5 to 9 dB over a 2.5–10 GHz frequency range. A comparison of measurement results with the prior published state-of-art UWB LNAs shows that our proposed linearized UWB LNA achieves excellent linearity with much less power than previously published works.

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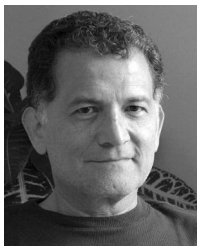

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