Design and Analysis of a High Efficiency DC-DC Converter with Soft Switching Capability for Renewable Energy Applications Requiring High Voltage Gain

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***Abstract*— Renewable sources like solar PV and fuel cell stack is preferred to be operated at low voltages. For applications such as grid tied systems, this necessitates high voltage boosting resulting in efficiency reduction. To handle this issue, this paper proposes a novel high voltage gain, high efficiency dc-dc converter based on coupled inductor, intermediate capacitor and leakage energy recovery scheme. The input energy acquired from the source is first stored in the magnetic field of coupled inductor and intermediate capacitor in a lossless manner. In subsequent stages it is passed on to the output section for load consumption. A passive clamp network around the primary inductor ensures the recovery of energy trapped in the leakage inductance, leading to drastic improvement in the voltage gain and efficiency of the system. Exorbitant duty cycle values are not required for high voltage gain, which prevents problems such as diode reverse recovery. Presence of a passive clamp network causes reduced voltage stress on the switch. This enables the use of low voltage rating switch (with low "on-state" resistance), improving the overall efficiency of the system. Analytical details of the proposed converter and its hardware results are included.**

***Keywords*— DC-DC Power Converter, Power Conditioning, Coupled Inductor, Switched Capacitor, Active Clamp, Passive Clamp, High Voltage Gain, Solar Photovoltaics.**

I. INTRODUCTION

In the last few decades, there has been a drastic increase in the demand for electricity. This has led to rapid use and depletion of fossil fuels. These factors have led the researchers to renewable energy sources such as wind, solar PV and fuel cell stack. Solar Photovoltaic (PV) and fuel cell energy sources play a prominent role among the existing renewable sources poses major challenges such as:

(a) Optimal utilization of the source due to their non-linear characteristics (e.g. Maximum Power Point Tracking (MPPT) is required to track maximum available power from a PV source);

(b) They are usually operated at low output voltage levels (typ. 25-50V) because of safety issues. This makes their application to grid connected systems and even some stand-alone loads difficult because a large voltage boosting is required.[1]

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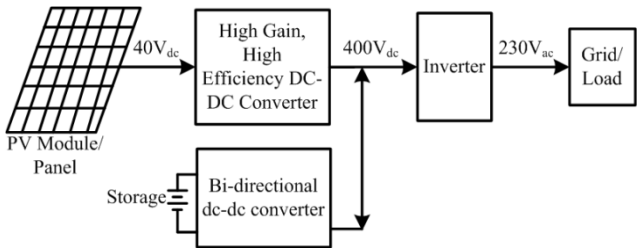


Fig. 1 Block diagram of a PV power conversion system

A direct implication of points (a) and (b) is that the use of a dc-dc converter [1,2] is essential at the front end, right across the source as shown in Fig. 1. Use of conventional dc-dc converters has the following disadvantages:

1. It causes large peak current to flow on the input side, which adversely affects the magnetic components and results in high losses.
2. It causes large voltage to appear across the switch. As the on state resistance of a switch depends on its voltage rating [$R_{DS(on)} \propto V_{DS}^2$], the conduction losses increase. Due to large duty cycle, the losses in parasitic resistances of inductance and capacitance also increase.
3. Diode reverse recovery becomes a major concern.

In view of the above, there is clearly a need to develop and use special high gain, high efficiency dc-dc converters to implement MPPT and to step up voltage level. Several circuit topologies have been proposed in the past [3-6] for this application. They follow one or more of the following philosophies to achieve high voltage at the converter output.

(a)Direct voltage step-up using high frequency transformer.

(b) Use of coupled inductor to utilize the energy storage capability of the magnetizing inductance of the core to increase the voltage level using turns ratio of the coupled inductor.

(c) Use of interleaved coupled inductor that facilitates use of smaller inductors, division of current and higher effective inductance for higher power applications.

(d) Active and passive clamp circuits to recover leakage energy in the coupled inductor based high gain converters to reduce losses in leakage inductance.

(e) Use of intermediate energy storage capacitors as additional buffers to increase the voltage gain without increasing duty cycle to high value.

A brief overview of the high voltage gain topologies reported in the literature is presented in the next section.

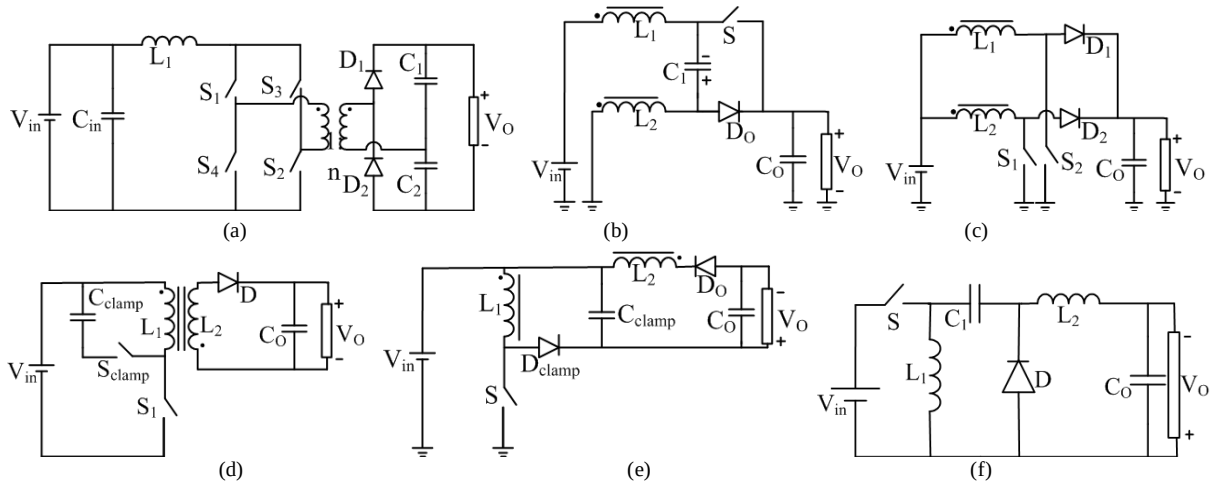


Fig. 2 Circuit diagrams of the high voltage gain dc-dc converters: (a) Isolated current-fed boost converter[8]; (b) Coupled inductor boost converter [11]; (c) Interleaved coupled inductor boost converter [14]; (d)Active clamp converter [9]; (e)Passive clamp converter [4]; (f) Intermediate Energy storage capacitor based converter [18].

II.OVERVIEW OF HIGH VOLTAGE GAIN DC-DC CONVERTER TOPOLOGIES

The converters shown in Fig. 2 depict some of the high voltage gain topologies that are representative of the existing configurations. Direct voltage step up using high frequency transformer renders a simple and easily controllable converter providing high gain. Isolated current-fed dc-dc converters [Fig. 2(a), [7-9] are example of this category. However these topologies result in high voltage spikes across the switch (due to leakage inductance) and large ripple in primary side transformer current as the turns ratio in the high frequency transformer increases. The isolated systems are relatively costly, bulky and generally less efficient [10] even though they offer more safety, eliminate issues such as ground leakage current and can provide multiple outputs among other advantages.

Most of the non-isolated high voltage gain dc-dc power converters employ coupled inductor (to achieve higher voltage gain) [Fig. 2(b)] [11] in contrast to a high frequency transformer used by the isolated versions [Fig. 2(a)]. The coupled inductor based dc-dc converter has advantages over isolated transformer based dc-dc converter in minimizing current stress, using lower rating components and simple winding structure. Modeling procedure of the coupled inductor is described in [12]. For high power converter applications interleaved coupled inductor based boost converters [13-15] have also been proposed [Fig. 2(c)].

A demerit of coupled inductor based systems is that they have to deal with higher leakage inductance, which causes voltage spikes across the main switch during turn-off time and current spike during turn-on time, resulting in a reduction of the overall circuit efficiency. The effects of leakage inductance can be eliminated by using an active clamp network shown in Fig. 2(d) [9,15], which provides an alternate path to recover leakage energy. But active clamp network is not as efficient as a passive clamp because of conduction losses across the power switch of the active clamp [16] network. Active clamp network consists of a switch with passive components while passive clamp network [Fig. 2(e)] [4] consists of passive components such as diode, capacitor and resistor. The passive clamp circuit is more popular to reduce voltage stress across the converter switch by recycling leakage energy [17].

The energy recovered from the leakage inductance can be calculated from the following equation:

$$\frac{1}{2}L_{lk}I_L^2 \quad (1)$$

where L_{lk} is leakage inductance, I_L is the inductor current and L_m is the magnetizing inductance given by:

$$L_{lk} = (1-k)L; L_m = kL \quad (2)$$

k is the coupling coefficient and L is the inductance. Voltage across clamp capacitor, C, can be calculated from (1):

$$\frac{1}{2}L_{lk}I_L^2 = \frac{1}{2}CV_C^2 \quad (3)$$

where, C and V_C are the clamping capacitance and clamp voltage, respectively.

Voltage gain of the converter can be increased without increasing the duty cycle of the switch by connecting an intermediate capacitor in series with the inductor [Fig. 2(f)][6,18,19]. The intermediate energy storage capacitor with coupled inductor charges in parallel and discharges in series with the coupled inductor secondary.

Various principles discussed in preceding paragraphs have also been used in combinations to achieve high voltage gain and enhanced features [20]. A coupled inductor type boost converter has been used in association with a passive clamp circuit to achieve high gain and increased efficiency [4]. Converter configurations with coupled inductor in association with a voltage multiplier circuit [21] and/or intermediate capacitor [22,23] have also been reported to achieve high voltage gain. In recent times, use of coupled inductors along with intermediate capacitors has also become popular [19].

Keeping in mind the merits and demerits of the various schemes described in preceding paragraphs, a novel topology has been proposed in this paper that achieves high voltage through a coupled inductor connected in interleaved manner that charges an intermediate buffer capacitor and a passive clamp network to recover the leakage energy. Coupled inductor leads to the

incorporation of 'turns ratio' into the gain expression that leads to high efficiency without increasing the duty ratio. As compared to existing high gain dc-dc converters, the number of passive components used in the proposed converter is less, which reduces the cost and improves the efficiency. Though the proposed converter is applicable to any low voltage source application (e.g. solar PV, Fuel cell stack, battery etc.), this paper focuses only on the solar PV source. All the details of this work are presented in the subsequent sections of the paper.

III. DESCRIPTION OF THE PROPOSED CONVERTER

Energy conversion efficiency of solar PV is quite low (about 12–25%) [24]. Therefore, it is essential to use a highly efficient power conversion system to utilize the PV generated power to the maximum. The proposed high gain dc-dc converter configuration is shown in Fig. 3. It consists of one passive clamp network, a coupled inductor (L_1,L_2) and an intermediate capacitor apart from other components.

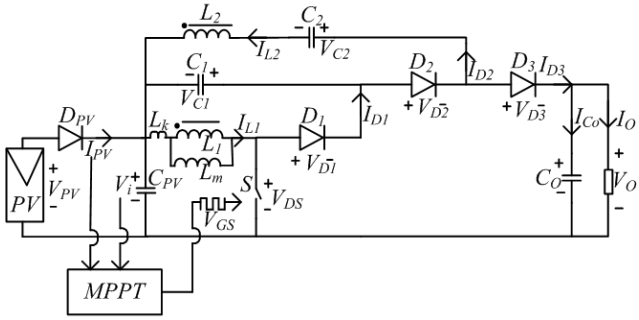
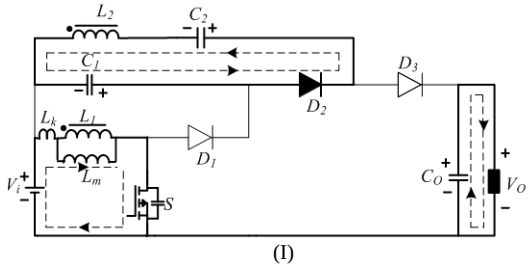
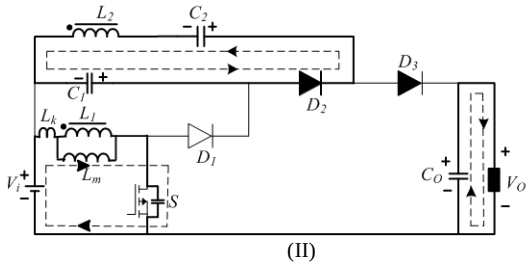


Fig. 3 Circuit diagram of proposed dc-dc converter

The symbol V_{PV} represents the PV voltage applied to the circuit. *S* is the main switch of the proposed converter. The coupled inductor's primary and secondary inductors are denoted by L_1 and L_2. C_1 and D_1 represent the passive clamp network across L_1. The capacitor C_O is the output capacitor while D_3 is the output diode. The voltage V_O is the average (dc) output across the load. The intermediate energy storage capacitor, C_2 and the feedback diode D_2 are connected on the secondary side.



(I)



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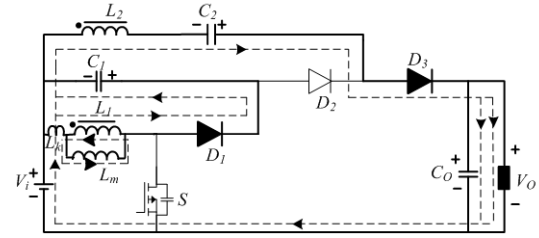
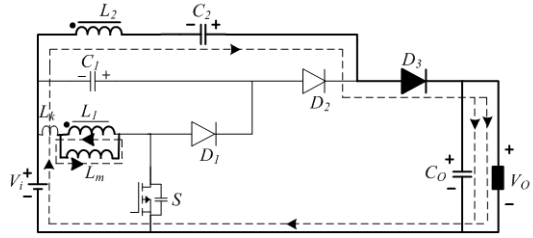
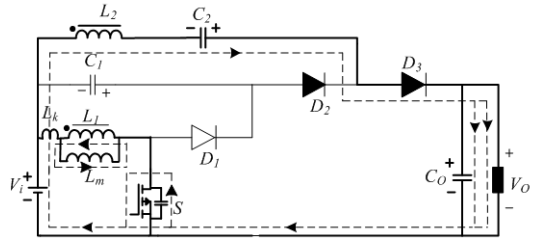


(III)



(IV)



(V)

Fig. 4 Various modes of opération during CCM: (I) Mode 1; (II) Mode 2; (III) Mode 3; (IV) Mode 4 ; (V) Mode 5.

The gain ratio, *n* is given by:

$$n = \frac{V_{L2}}{V_{L1}} \tag{4}$$

where, V_{L1} and V_{L2} represent the voltages across inductors L_1 and L_2. The operating modes for continuous conduction mode (CCM) are shown in Fig. 4. Various operating modes are described below:

Mode 1[t_0-t_1]: The switch (*S*) is turned on at the start of the converter operation. The current flows through the switch and the primary side of the coupled inductor (L_1), energizing the magnetizing inductance (L_m) of the coupled inductor. The current path is as shown in Fig. 4(I). The two diodes, D_1 and D_3 are reverse biased, while D_2 is forward biased during this mode. The intermediate capacitor, C_2 is charged through D_2 by L_2 and capacitor, C_1. If voltage across intermediate capacitor (C_2) becomes equal to the summation of voltages across L_2 and C_1, diode D_2 turns off. The current flowing through L_m (i_{Lm}) in this mode may be obtained by using the following relation:

$$i_{Lm}(t) = \frac{V_i}{L_m + L_k}(t - t_0) + i_{Lm}(t_0) \tag{5}$$

The parasitic capacitance of the switch *S* is charged by the magnetizing current flowing through the inductor L_1. The diode D_2 remains forward biased and current continues to flow through this. Current path in this mode is shown in Fig. 4(II).The magnetizing inductance current for this mode is given by the following equation:

$$i_{Lm}(t) = \frac{V_i}{L_m + L_k}(t - t_1) + i_{Lm}(t_1) \tag{6}$$

Mode 3[t_2-t_3]: In this mode, diodes D_1 and D_3 become forward biased. D_2 is reverse biased and its current becomes zero in this mode. The leakage energy stored in

the primary side of the coupled inductor (L_1) is recovered and stored in the clamp capacitor (C_1) through D_1. Also, the energy is transferred from the input side to the output side through diode D_3 as shown in Fig. 4(III). The recovered leakage inductance current (i_{Lk}) is given by:

$$i_{Lk}(t) = \frac{V_{C1}}{L_m+L_k}(t-t_2) + i_{Lm}(t_2) \quad (7)$$

Mode 4[t_3-t_4]: This mode begins after the completion of recovery of the leakage energy from inductor L_1. The diode D_1 now becomes reverse biased while diode D_3 remains forward biased in this mode. The current flows from the input side to the output side to supply the load as shown in Fig. 4(IV). The current i_{Lm} flowing through secondary inductor (L_2) is given by the following equation:

$$i_{Lm}(t) = \frac{(V_0-V_{C2}-V_i)}{nL_m}(t-t_3) + i_{Lm}(t_3) \quad (8)$$

Mode 5[t_4-t_0]: This mode begins by turning on switch *S*. The leakage inductor energizes quickly using the full magnetizing current while the parasitic capacitance across the switch discharges in this mode. The two diodes D_1 and D_2 are in reverse biased condition. The current flow path in this mode is shown in Fig. 4(V). This mode ends when diode D_3 becomes reverse biased and current flow through inductor, L_2 changes direction. The secondary inductor current (i_{Lm}) continues to flow in this mode and current is given by:

$$i_{Lm}(t) = \frac{(V_0-V_{C2}-V_i)}{nL_m}(t-t_4) + i_{Lm}(t_4) \quad (9)$$

Since the current through an inductor ($i_{lk} = \frac{V_i(t-t_4)}{(L_m+L_k)}$) cannot change instantaneously, current rises slowly. The voltage (V_{DS}) across the switch 'S' cannot change instantaneously and decreases slowly. Thus, there is little overlap of falling voltage and rising current and negligible switching loss at turn-on.

Typical waveforms of the circuit are shown in Fig. 5.

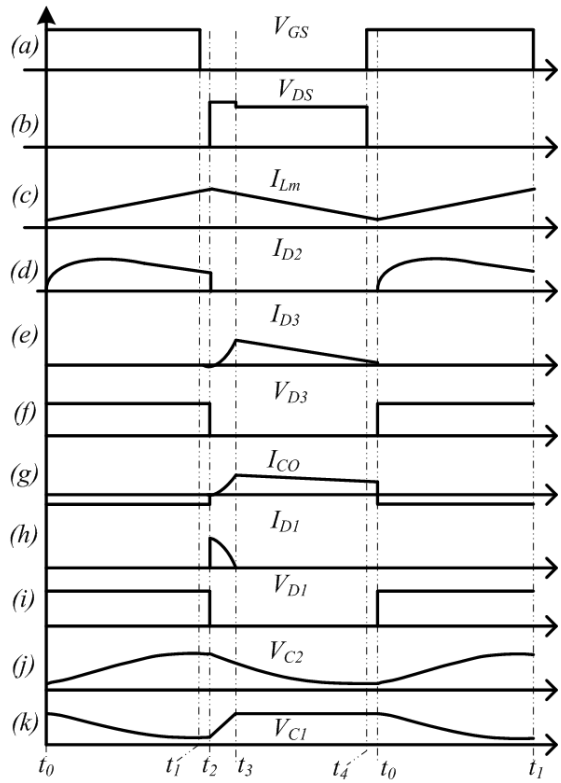


Fig. 5 Typical waveforms during CCM operation.

IV. ANALYSIS AND DESIGN

This section presents the analysis of the proposed converter which can be used for its design.

All the elements used in the converter are assumed to be ideal.

When Switch S is ON: The voltage across L_1 is given by:

$$V_{L1(ON)} = V_i \quad (10)$$

The voltage across L_2 is given by:

$$V_{L2} = V_{C2} - V_{C1} \quad (11)$$
$$V_{L2} = nV_i$$

When Switch S is OFF: The voltage across L_1 is given by:

$$V_{L1(OFF)} = -V_{C1} \quad (12)$$

Applying Kirchoff's voltage law in Mode 3 yields:

$$V_{L2} = V_i + V_{C2} - V_o \quad (13)$$

By substituting V_{C2} from (11) and (12) into (13), it becomes: $V_{L2} = V_i - V_{L1(OFF)} + nV_i - V_o$ (14)

$$\text{Also, } V_{L1} = \frac{V_{L2}}{n} \quad (15)$$

By substituting (14) into (15), voltage expression during switch off condition becomes:

$$V_{L1(OFF)} = \frac{(V_i - V_{L1(OFF)} + nV_i - V_o)}{n}$$

$$\text{or, } V_{L1(OFF)} = \frac{(V_i+nV_i-V_o)}{(n+1)} \quad (16)$$

Voltage Gain: By applying voltage-sec balance across L_1:

$$V_{L1(ON)}d + V_{L1(OFF)}(1-d) = 0 \quad (17)$$

Substituting values of $V_{L1(ON)}$ and $V_{L1(OFF)}$ from (10) and (16) respectively into (17) yields:

$$V_i d + \frac{(V_i+nV_i-V_o)}{(n+1)}(1-d) = 0$$
$$\frac{V_o}{V_i} = \frac{(n+1)}{(1-d)} \quad (18)$$

Substituting (18) into (16) results in:

$$V_{L1(OFF)} = -\frac{d}{(1-d)}V_i \quad (19)$$

Switch voltage: Voltage across the switch during OFF time is given by:

$$V_{DS} = -V_{L1(OFF)} + V_i \quad (20)$$

Substituting (19) into (20) results in:

$$V_{DS} = \frac{d}{(1-d)}V_i + V_i \quad (21)$$

$$V_{DS} = \frac{V_i}{(1-d)} \quad (22)$$

Again, the voltage across the clamp capacitor, C_1 is nearly constant for the entire switching period. Using (12) and (19):

$$V_{C1} = \frac{d}{(1-d)}V_i \quad (23)$$

Intermediate Capacitor Voltage (V_{C2}): The voltage across intermediate energy storage capacitor would be nearly constant (negligible ripple) and can be determined from (11) as follows:

$$V_{C2} = V_{C1} + V_{L2} \quad (24)$$

By substituting (13) and (23) in (24):

$$V_{C2} = \frac{d}{(1-d)} V_i + nV_i \quad (25)$$

$$V_{C2} = \frac{d(1-n)+n}{(1-d)} V_i \quad (26)$$

Reverse bias voltage across diodes (V_{D1}, V_{D2}, V_{D3}):
Voltage across diode (D_1):

$$V_{D1} = V_{L1(ON)} + V_{C1} \quad (27)$$

By substituting (10) and (23) into (27), the voltage across diode, D_1 becomes:

$$V_{D1} = \frac{V_i}{(1-d)} \quad (28)$$

Voltage across diode (D_2) is:

$$V_{D2} = V_{L2} + V_{C2} - V_{C1} \quad (29)$$

By substituting (13), (23) and (26) in (29), it becomes:

$$V_{D2} = 2nV_i \quad (30)$$

Voltage across diode D_3:

$$V_{D3} = V_{L2} - V_{C2} - V_i + V_o \quad (31)$$

By substituting the value of V_{L2} from (13), V_o from (18) and V_{C2} from (26) in (31) yields:

$$V_{D3} = \frac{n}{(1-d)} V_i \quad (32)$$

Magnetizing Inductance (L_m): $L_m = \frac{1}{2} \times \frac{V_i \times d}{d \times I_{Lm} \times f_s}$ (33)

Forward Bias Diode Currents (I_{D1}, I_{D2}, I_{D3}):
Current flow through diode D_1 can be derived as follows:

$$L_1 \frac{dI_{D1}}{dt} = V_{C1}$$

$$I_{D1} = \frac{V_{C1} \times d_{lk}}{L_1 \times f_s} \quad (34)$$

where $d_{lk}T_S$ is the period during which the leakage energy is transferred. Current flowing through diode D_2 can be calculated as below (S ON):

$$L_2 \frac{dI_m}{dt} = V_{C2} - V_{C1}$$

where, $I_m = nI_{L2}; I_{L2} = I_{D2}$

$$\therefore \quad I_{D2} = \frac{(V_{C2} - V_{C1}) \times d}{n \times L_2 \times f_s} \quad (35)$$

Similarly, the current flowing through diode D_3 can be calculated as below (S OFF):

$$L_2 \frac{dI_m}{dt} = V_o - V_{C2} - V_i$$

where, $I_m = nI_{L2}; I_{L2} = I_{D3}$

$$\therefore \ I_{D3} = \frac{(V_o - V_{C2} - V_i)(1-d-d_{lk})}{n \times L_2 \times f_s} \quad (36)$$

Presence of leakage inductance in the circuit manifests itself in the following manner:

$$V_i = L_m \frac{di}{dt} + L_k \frac{di}{dt} \quad (37)$$

Then current flowing through inductor becomes:

$$i = \int \frac{V_i}{(L_m + L_k)} dt \quad (38)$$

From (38), it is clear that the current flowing through the circuit is reduced if leakage inductance is present.

Also, $V_{L1} = kV_i$ (39)

where, k is the coupling coefficient of the coupled inductor.

$$V_{L1} = knV_i \quad (40)$$

By using (10)-(18) and taking into account the leakage inductance, voltage gain expression can be determined as:

$$\frac{V_o}{V_i} = \frac{(nk+1)+d(k-1)}{(1-d)} \quad (41)$$

V. EXPERIMENTAL RESULTS

The high gain dc-dc converter, shown in Fig. 3, is implemented in hardware in order to validate its operational principle as explained in section III. A set of experimental plots obtained from this laboratory prototype are included in this section. Texas Instruments' controller '*PICCOLO F28069*' has been used to control the proposed dc-dc converter. The details of the components used for the experiments with the laboratory prototype of the proposed dc-dc converter are given in Table I.

TABLE I
LIST OF COMPONENTS

S	FDH055N15A (150V /167 A, $R_{DS(ON)}$ = 4.8mΩ)[2]
D_1 D_2 D_3	BYC20X-600(t_{rr}=35nS) DPG20C300PB (t_{rr}=35nS) CSD01060
C_O	400V/180μF Ceramic caps
C_2	250V/47μF
C_1	63V/1μF
Coupled Inductor	Cosmo ferrite core with L_m=50uH DC resistance Primary=70mΩ DC resistance Secondary=300mΩ

The system specifications of the proposed converter developed in the lab are given in Table-II.

TABLE II
SPECIFICATIONS OF THE LABORATORY PROTOTYPE CONVERTER

Rated Power	400W
Input DC Voltage	25-50V
Output Voltage	(400-500)V
Turns ratio of the coupled Inductor (n)	4
Switching Frequency (f_s)	50kHz

Design Procedure: For the given input, output specifications, a suitable turns ratio is selected [Table II] and the nominal duty cycle can then be calculated using (18). The value of the magnetizing inductance (L_m) can be derived from (10) as [25]:

$$L_m = \frac{V_i d}{2\Delta I_m f_s} \quad (42)$$

[2] As the boost converter switch has to bear much higher voltage, a higher voltage switch (MOSFET FCH47N60N, R_{ON}=0.068Ω) is used.

The minimum value of the clamp capacitor C_1 can be derived as follows:

$$C_1 = \frac{I_m d_{lk}}{\Delta V_{C1} f_s} \quad (43)$$

The minimum value of the intermediate capacitor C_2 can be derived as follows:

$$C_2 = \frac{I_m d}{n \Delta V_{C2} f_s} \quad (44)$$

The minimum value of the output capacitor C_o can be derived as:

$$C_o = \frac{I_o d}{\Delta V_o f_s} \quad (45)$$

The output voltage ripple in (45) includes ripple due to the presence of parasitic resistance of the output capacitor and duration of the holding time during transients of the switch [26] as per the following equation:

$$\Delta V_o = \Delta V_{Co} + r_{co} \quad (46)$$

where, r_{co} is the parasitic resistance of the capacitor C_o. Initially, we don't know the value of C_o. Hence, it is not possible to determine the value of r_{co}. For initial calculation it is assumed that $\Delta V_o = \Delta V_{Co}$ and voltage ripple is 1% of V_o. The value of output capacitor is derived as below:

$$C_o = \frac{I_o d T_s}{0.01 V_o} \quad (47)$$

and equation (46) becomes:

$$0.01 V_o = \Delta V_{Co} + r_{co} I_{co} \quad (48)$$

The minimum required value of output capacitance is derived as below:

$$C_{o(min)} = \frac{\Delta I_o x T_s}{0.01 V_o} \quad (49)$$

where, xT_s is the hold-up time for the load transient of ΔI_o. The value of x can vary from 10% to 50%.

TABLE III
KEY CIRCUIT VARIABLES AND COMPARISON BETWEEN ANALYTICAL AND HARDWARE RESULTS

Parameters	Formula	Analytical Results	Hardware Results
Voltage across C_1	$V_{C1} = \frac{d}{(1-d)} V_i$	*45V*	*45V*
Voltage across C_2	$V_{C2} = \frac{d(1-n)+n}{(1-d)} V_i$	*225V*	*224V*
Reverse voltage across D_1	$V_{D1} = \frac{V_i}{(1-d)}$	*90V*	*87V*
Peak current through D_1	$I_{D1} = \frac{V_{C1} \times d_{lk}}{L_1 \times f_s}$	*7.2A*	*7A*
Reverse voltage across D_2	$V_{D2} = 2nV_i$	*360V*	*350V*
Peak current through D_2	$I_{D2} = \frac{(V_{C2} - V_{C1}) \times d}{n \times L_2 \times f_s}$	*2.25*	*2.5A*
Reverse voltage across D_3	$V_{D3} = \frac{n}{(1-d)} V_i$	*360V*	*350V*
Peak current through D_3	$I_{D3} = \frac{(V_o - V_{C2} - V_i)(1-d-d_{lk})}{n \times L_2 \times f_s}$	*1.75A*	*1.85A*
Reverse voltage across switch S	$V_{DS} = \frac{V_i}{(1-d)}$	*90V*	*87V*
Peak Current through L_m	$I_{Lm} = \frac{V_i}{L_m} dT_s$	*9A*	*9.25A*
Peak current through L_1	$I_{L1} = \frac{n}{2} I_{Lm}$	*18A*	*18.5A*
Value of the magnetizing inductance	$L_m \geq \frac{1}{2} \times \frac{V_i d}{d \times I_L \times f_s}$	$L_m \geq 48\mu H$	*50μH*

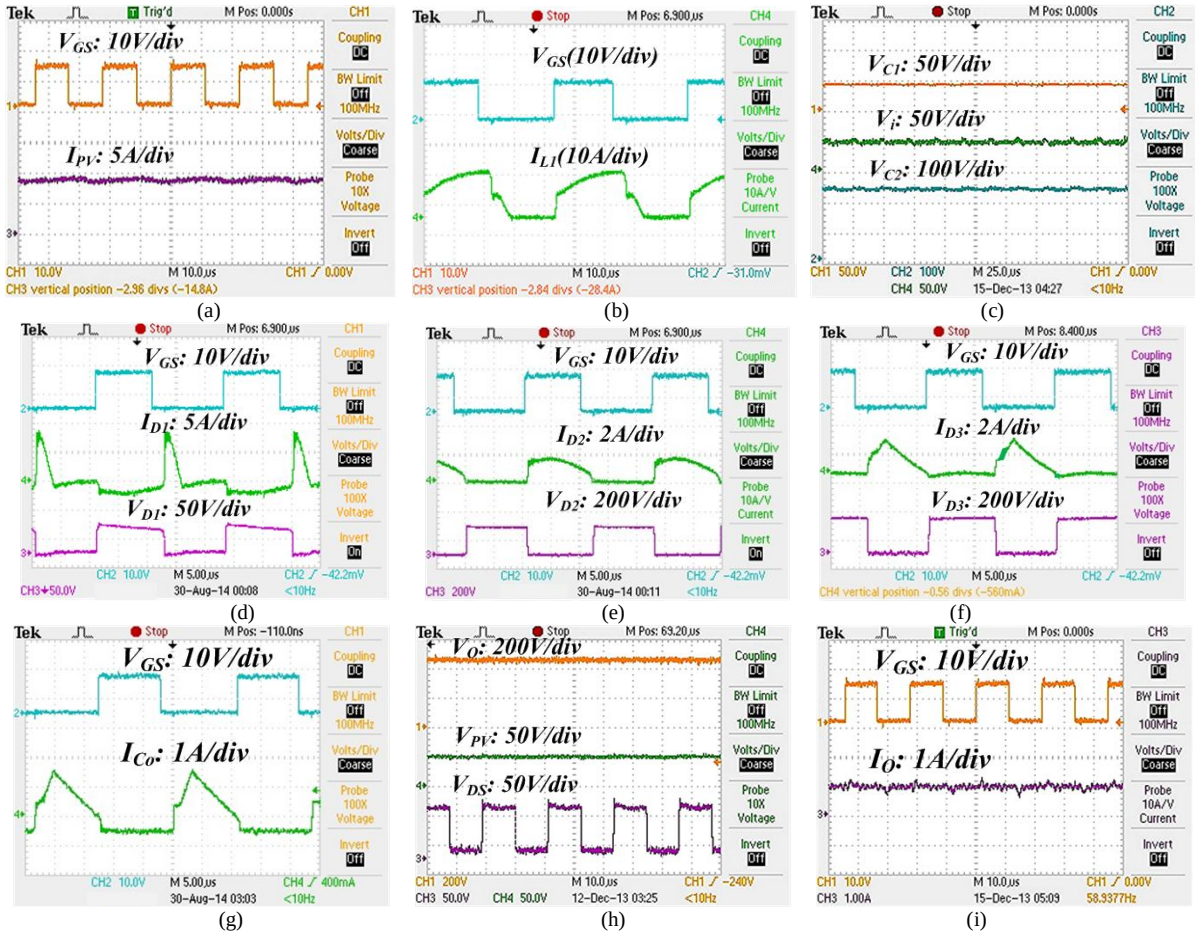


Fig. 6 Experimental results under full load (400W) conditions.

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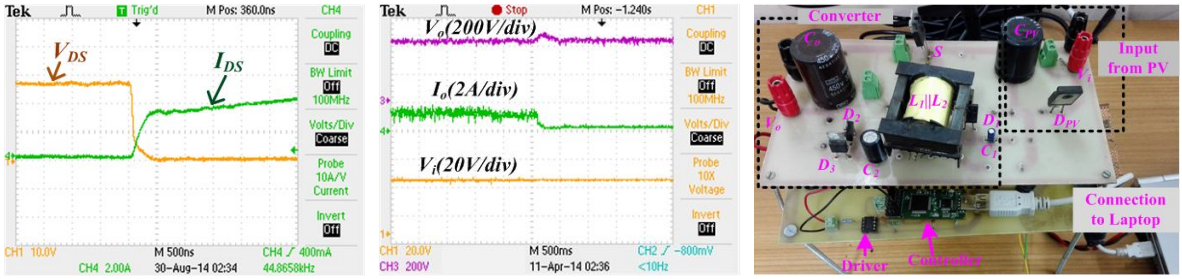


(a) (b) (c)

Fig. 7 (a) Low loss turn-on of the converter switch; (b) Transient response of the converter (400W to 40W); (c) Hardware prototype of the proposed converter.

All the voltage and current values are derived and calculated in Table III. Those values can be used for the selection of suitable MOSFET and diodes. The key circuit variables of the proposed converter prototype along with their expressions are given in Table III. For analytical calculations given in column 3 of Table III, $d=0.5$, $V_i=45V$, $n=4$ and $f_s=50kHz$ have been used. The hardware results shown in column 4 are for CCM operation and compare well with the steady state analytical calculations [column 2].

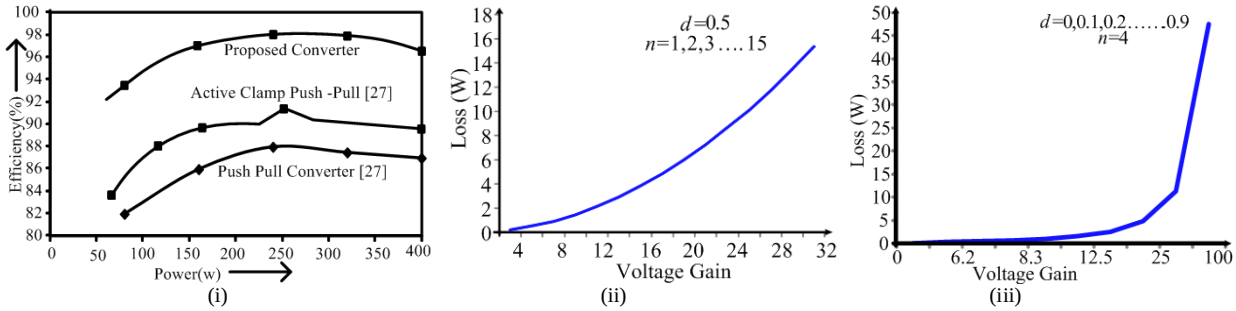
The experimental waveforms are shown in Fig. 6. These are the measured waveforms under full load (400W) conditions with MPPT. A 'TerraSAS' PV simulator is used as the PV source. For a given radiation level, the current drawn from the input PV source is nearly constant as shown in Fig. 6(a). The current flowing through primary of coupled inductor (L_1) is shown in Fig. 6(b). The voltage across clamp capacitor (C_1) and intermediate capacitor (C_2) with input buffer capacitor across PV are also nearly constant as shown in Fig. 6(c).The current and voltage waveforms of the clamp diode D_1 are shown in Fig. 6(d), which match with typical waveform I_{D1} shown in Fig. 5(h). The current and voltage of intermediate diode D_2 are shown in Fig. 6(e), which compare reasonably well with Fig. 5(d). The current and voltage waveforms of the output diode (D_3) are shown in Fig. 6(f). The nature of current through the output filter capacitor is shown in Fig. 6(g), which compares well with the typical simulation waveform shown in Fig. 5(g). According to the calculation V_{DS} is ≈80V for a 450V output voltage, which matches closely with Fig. 6(h). The output current of the converter is shown in Fig. 6(i).

An interesting benefit of the proposed converter is that it incurs "low loss switching" during turn ON, without any extra circuit arrangement. The leakage energy is recycled by the passive clamp circuit. So, the current flowing through the switch starts from zero during turn ON. Experimental verification of low loss switching feature of the proposed converter is depicted in Fig. 7(a), which makes turn-ON losses almost zero. The result shown in Fig. 7(b) is for a load step down from 400W to 40W, to show transient stability of the converter. The output voltage of the converter is stable even with the change of load from 100% to 10%. A picture of the experimental prototype is shown in Fig. 7(c).

Efficiency plot with respect to load variation of the proposed converter is shown in Fig. 8(i). The efficiency plot of the proposed converter is compared with conventional push-pull converter having identical input-output voltage ratings (V_i=40V; V_o=400V) and operating frequency (50kHz). Full load (400W) efficiency of the converter, obtained from experimentation, is 96% (maximum ≈97% at lighter load). A comparison is also shown with conventional, hard switched push pull converter (of identical rating, operating frequency and input/output voltage specifications) with and without active clamp across the main switch. The proposed system shows a higher efficiency under all load conditions. Fig. 8(ii) shows a plot of gain versus losses by varying the turns ratio of the coupled inductor while duty cycle of the dc-dc converter is held constant at 0.5. Fig. 8(iii) shows the gain versus loss curve as the duty cycle of the dc-dc converter is varied (with turns ratio of the coupled inductor held constant at 4).

VI. CONCLUSIONS

The high gain, high efficiency converter proposed in this paper is highly suitable for low output voltage sources (e.g. solar PV, Fuel Cell Stack, Battery).



(i) (ii) (iii)

Fig. 8 (i) Efficiency versus load curve for the proposed dc-dc converter and comparison with existing versions; (ii) Loss versus gain plot by varying voltage gain with the variation of turns ratio (n), keeping duty cycle (d) constant; (iii) Loss versus gain plot by varying voltage gain with the variation of d, keeping n constant.

A circuit efficiency of 96% is achieved under full load conditions. Table III provides a comparison of the key circuit variables values obtained analytically with hardware measurements. The error in the results between analytical derivation and experimental results [Fig. 6] is found to be between 0 to 5%. This could be attributed to measurement errors, presence of parasitics and use of imprecise values of circuit components for experimentation. The trend shown in the plots of Figs. 8(ii) and 8(iii) suggests that a good way to design and use the proposed converter would be to use turns ratio of the inductor around 4 or 5 (fixed during the design) and vary the duty ratio from 0 to 0.7 while operating. Beyond this range of duty cycle and turns ratio, the losses become significantly higher. High voltage gain is achieved without using extreme duty cycle values, which is a big advantage over conventional step-up converters. One of the reasons for high efficiency in the proposed converter is reduction in the switching loss during turn-on due to low loss switching. Table IV provides a comparison of the key circuit parameters of a conventional boost converter with proposed high gain converter for identical applications and specifications.

Looking at these numbers, the superior performance of the proposed converter is quite evident. The Euro efficiency and CEC efficiency [28] for the proposed converter are obtained as follows:

Euro Efficiency = (0.03×90% + 0.06×93% + 0.13×95% + 0.1×96% + 0.48×97%+ 0.2×96%) = 96%

CEC Efficiency = (0.04×90% + 0.05×93%+ 0.12×95% + 0.21× 96% + 0.53× 97% + 0.05× 96%) = 96.02%

TABLE IV
COMPARISON WITH CONVENTIONAL BOOST CONVERTER

	Boost Converter *($d=0.9, V_i=45V, f_s=50kHz$,* MOSFET FCH47N60N, *$R_{ON}=0.068\Omega$, $L=50uH$, $C=4.7uF$)*	Proposed Converter *($d=0.5, f_s=50kHz$, $V_i=45V$, $n=4$,* MOSFET FDB86135, *$R_{ON}=0.0035\Omega$, $L=50uH$, $C=4.7uF$)*
Voltage gain	$\frac{V_o}{V_i}=\frac{1}{(1-d)} \Rightarrow 450V$	$\frac{V_o}{V_i}=\frac{(n+1)}{(1-d)} \Rightarrow 450V$
Switch loss	$R_{ON_{sw}} \times d \times \left(\frac{I_{out}}{(1-d)}\right)^2 \Rightarrow 6.12W$	$R_{ON_{sw}} \times d \times \left(\frac{(n+1)}{(1-d)} I_{out}\right)^2 \Rightarrow 0.18W$
Inductor loss	$r_L \times \left(\frac{I_{out}}{(1-d)}\right)^2 \Rightarrow 100 r_L$	$r_L \times \left(\frac{(n+1)}{(1-d)} I_{out}\right)^2 \Rightarrow 100 r_L$
Switch voltage drop(V_{DS})	$\frac{V_i}{(1-d)} \Rightarrow 450V$	$\frac{V_i}{(1-d)} \Rightarrow 90V$
Current through Inductor	$\frac{V_i}{L} dT_s \Rightarrow 18A$	$\frac{V_i}{L} dT_s \Rightarrow 9A$
Leakage energy $C = C_{snubber}$	$\frac{1}{2} C \left(\frac{V_i}{(1-d)} d\right)^2 \Rightarrow 0.38W$	$\frac{1}{2} C \left(\frac{V_i}{(1-d)} d\right)^2 \Rightarrow 0.004W$
Switch current	$I_{sw} = I_L = I_{in} \Rightarrow 18A$	$I_{sw} = I_L = (I_{in} - \frac{I_{L2}}{n}) \Rightarrow 9A$

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