A CLASS A/B LOW POWER AMPLIFIER FOR WIRELESS SENSOR NETWORKS

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ABSTRACT

In a dense ad-hoc wireless sensor network, the transmit power is comparable to the circuit power. Linear power amplifiers, which require lower drive power as compared to its switching counterparts, now become a viable candidate. This paper presents a class A/B low power amplifier suitable for ad-hoc wireless sensor network. The amplifier is implemented in 0.13µm CMOS process and operates with nominal 1.2V supply. Capacitive transformer is used to match the antenna to power amplifier for maximum efficiency. The amplifier achieves 35% drain efficiency while delivering 2.6mW at 1.92 GHz. With 1.5V supply, the power amplifier delivers 4.8mW with 38% drain efficiency.

1. INTRODUCTION

Ad-hoc wireless sensor networks such as Picoradio [1,2] are emerging as a new untapped realm in wireless communications. These ubiquitous networks can be embedded into the fabric of our daily living environment, enabling a wide variety of applications such as smart buildings, interactive user interfaces, environment control, warehouse inventory and home automation. Regardless of the specific usage, these high volume consumer applications all share the need for an ultra-low power, low cost and low form factor short-range transceivers.

A key component in ad-hoc wireless network transceivers is the low power amplifier. Due to the distributed nature of ad-hoc sensor networks, the low power amplifier faces very different design challenges as compared to its counterparts in traditional transceivers (e.g. Wireless LAN, Bluetooth) [3]. In a typical sensor network, the transmitter sends out sporadic bursts of short data packets (aggregate data rate ~ 10kbits/sec) to neighboring sensor nodes (< 10m). To reduce operational cost, all the energy used by the transceiver is either scavenged from the environment [4] or from a battery source [5] and it should last the entire lifetime of the product. This could be multiple years for applications such as smart homes. With today's energy generation technologies and reasonable node size, an average power dissipation of around 100 µW is realistic [6]. Energy being the most precious resource in a sensor node means that (1) the power added efficiency of the power amplifier when switched on should be maximized, (2) power control mechanism should be incorporated to vary the output power for various transmit distance, (3) the power amplifier should be shutdown when idle, (4) the turn-on time of the power amplifier should be short to minimize overhead power, and (5) the transmit power should be about 1-3mW for typical receiver sensitivity and indoor multi-path fading conditions.

This paper presents the design, implementation and results of a class A/B low power amplifier suitable for ad-hoc wireless sensor networks. Although linear power amplifiers generally have lower drain efficiency than switching amplifiers (Class D, E and F), they require lower drive power [7]. This is especially important in the case of low transmit power (1-3mW), where the transmit power is comparable to the circuit power. Thus linear amplifiers remain competitive from the perspective of overall transmitter efficiency. In addition, they allow for easier implementation of power control, more complex modulation schemes (e.g. QAM), and concurrent transmissions to neighboring nodes.

The first part of the paper focus on the design issues and explains the trade offs. Next, simulated and measured results are discussed. Finally, the last section concludes this paper.

2. DESIGN CONSIDERATIONS

The schematic and circuit waveforms of the low power amplifier are shown in Fig. 1.

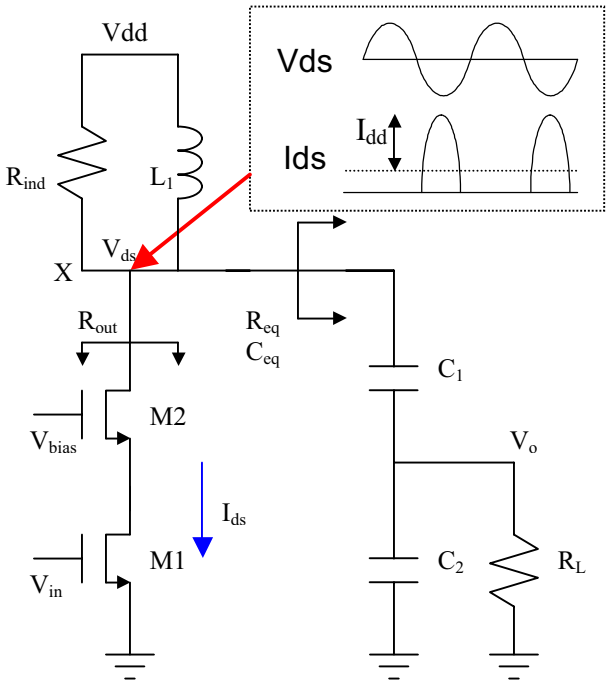

Fig 1: Circuit schematic. Inset shows the circuit waveforms

The circuit operation is as follows. Transistor M1 operates as a trans-conductor and converts its input voltage signal V_{in} into drain current I_{ds}. The RF tank, formed by inductor L_1 and all the capacitances at node X, filters out the harmonics in the drain current and only allows the fundamental drain current to flow to the resistances seen at node X, resulting in sinusoidal drain voltage V_{ds}. The fundamental component of the drain current I_1, DC current I_{dc} and the output power P_{out} are given as [8]

$$I_1 = \frac{I_{dd}}{\pi}(\sin y - y\cos y), \tag{1}$$

$$I_{dc} = \frac{I_{dd}}{2\pi}(2y - \sin 2y), \tag{2}$$

$$P_{out} = \frac{1}{2} I_1^2 \left(\frac{R_{ind} // R_{out}}{R_{ind} // R_{out} + R_{eq}} \right)^2 R_{eq} \tag{3}$$

where 2y is the conduction angle, R_{out} is the output resistance of the cascoded transistors, R_{ind} is due to the finite inductor Q-factor, V_{ds} is the sinusoidal drain voltage at node X and I_{dd} zero to peak drain current if the conduction angle is π.

The drain efficiency η of the amplifier is thus given as:

$$\eta = \frac{P_{out}}{P_{dc}} \tag{4a}$$

$$= \frac{1}{2}\left(\frac{I_1}{I_{dc}}\right)\left(\frac{V_{ds}}{V_{dd}}\right)\left(\frac{R_{ind} // R_{out}}{R_{ind} // R_{out} + R_{eq}}\right)^2 \bullet \left(\frac{R_{eq}}{R_{ind} // R_{out} // R_{eq}}\right) \tag{4b}$$

$$= \frac{1}{2}\left(\frac{I_1}{I_{dc}}\right)\left(\frac{V_{ds}}{V_{dd}}\right)\left(\frac{R_{ind} // R_{out}}{R_{ind} // R_{out} + R_{eq}}\right) \tag{4c}$$

To maximize the drain efficiency for a given output power, the output voltage swing V_{ds} and $R_{ind}//R_{out}$ have to be maximized. For a 1.2V supply, the maximum achievable swing is the DC drain voltage of M2 (~1.2V) minus the saturation voltage of M1 (~100mV). This translates to a transformed impedance of 504 Ω for an output power of 1.2mW if the loading due to R_{out} and R_{ind} are negligible. The required impedance matching is achieved by the capacitive transformer C_1 and C_2. Capacitive transformers are preferred over LC matching networks or inductive transformers because on-chip capacitors have much higher Q-factor (>50) than on-chip inductors (Q-factor of 5 to 10), resulting in less loss.

The impedance looking into the transformer Z_{eq} is given as:

$$Z_{eq} = \frac{1}{j\omega C_1} + \left(R_L // \frac{1}{j\omega C_2} \right) \tag{5}$$

C_1 and C_2 can be chosen to provide the required impedance. The equivalent capacitance C_{eq} and the parasitic capacitance at node X are used together with inductor L_1 to form the RF tank. By making C_1 and C_2 tunable to provide different transformed resistance but the same equivalent capacitance, certain discrete levels of power control are possible.

Another critical issue in power amplifier design using deep sub-micron devices is the low breakdown voltage of the gate oxide. To alleviate this problem, transistor M2 is cascoded on top of M1 and V_{bias} is chosen to ensure that the voltage across the gate does not exceed the maximum voltage rating of the process. In addition, cascoding increases the output impedance looking into the drain of M2, thus improving the efficiency. Also, transistor M2 improves the isolation between the input and output.

In our current design, the required inductance L_1 is 3.6nH. If L_1 is implemented using on-chip inductor with Q-factor

of 7, R_{ind} is about 304Ω. Even if R_{out} is infinite, the drain efficiency will be reduced by 62%, which is unacceptable. To solve this problem, inductor L_1 is implemented as a combination of a short bond wire inductor and an off-chip inductor connected in series. These inductors have much higher Q as compared to on-chip inductors, resulting in lower losses. An external inductor is used to mitigate the tolerance of the bond wire inductance. However, inductor L_1 can also be implemented solely using bond wire inductor if tuning capacitors are used at drain node X to account for the variations in the bond wire inductance or if the required length of the bond wire can be reproduced accurately by automated wire-bonder as in production environment.

3. RESULTS

The designed low power amplifier was fabricated in 0.13µm CMOS process from ST Microelectronics. The die is packaged to the test board (see Fig. 2) using Chip-on-board technology to reduce parasitic.

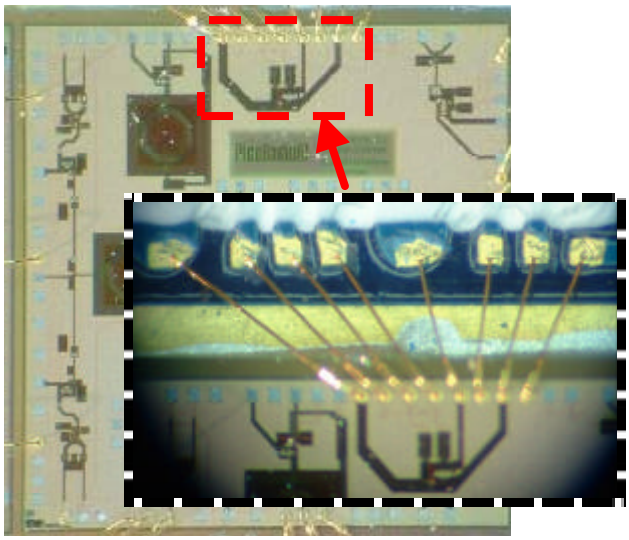

Fig. 2. Die photo. Inset shows packaged low power amplifier using chip-on-board technology.

The load power and dc power consumption are measured for various input drive powers at 1.2V supply voltage. The drain efficiency and power added efficiency (PAE) for various output power are plotted in Fig. 3. For output power more than 2.6mW, the drain efficiency is around 35%. A peak power added efficiency of 26% is achieved at output power of 2.6mW. At higher output power, power added efficiency degrades due to gain compression.

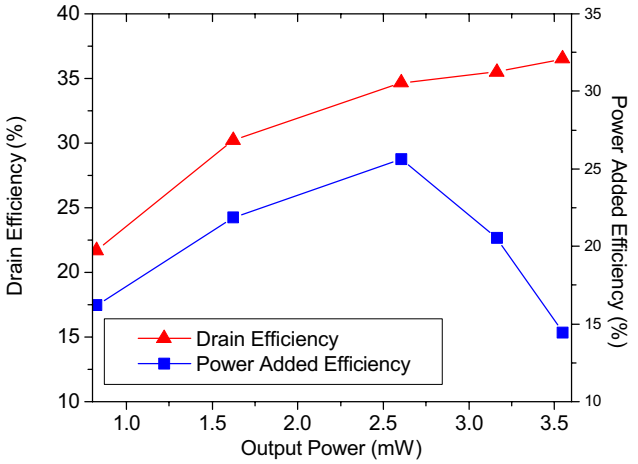

Fig 3. Drain efficiency and PAE at various output power.

The output power and drain efficiency are also measured at various supply voltages (see Fig. 4). The power amplifier operates with supply voltages ranging from 0.5V to 1.5. A peak drain efficiency of 38% is achieved with 4.8mW of output power at 1.5V supply. A plot of the output spectrum at 1.92 GHz is shown in Fig. 5.

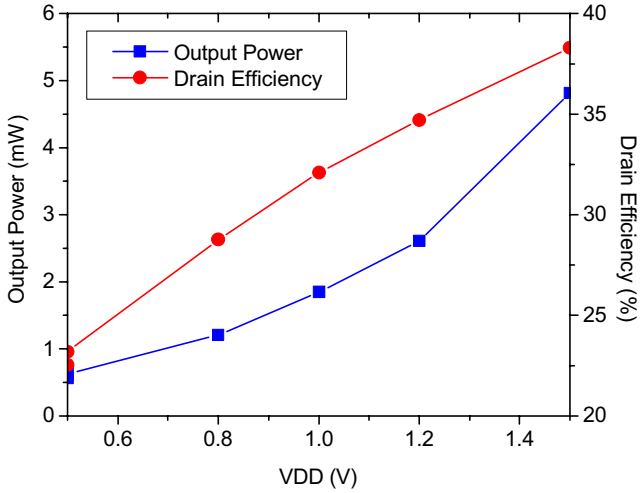

Fig 4. Output power and drain efficiency at various VDD.

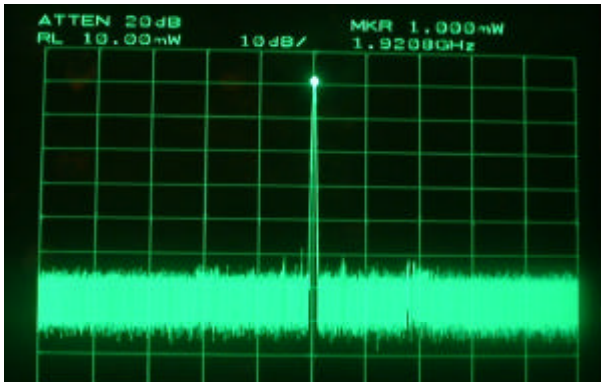

Fig 5. Output spectrum at 1.92 GHz

Fig. 6 shows a plot of the output power against the input power at 1.2V supply voltage. In a typical wireless sensor network transceiver, the drive power from the previous stage (oscillator or mixer) is around –10dBm to -4dBm. For a low transmit power of 1mW, a power gain of 6dB to 10dB is sufficient. The measured power gain is about 6dB. The lower than expected power gain is due to board parasitic. Thus, the power gain is expected to be higher when integrated in a transceiver. The 1-dB compression point occurs when the input power is –3.5dBm.

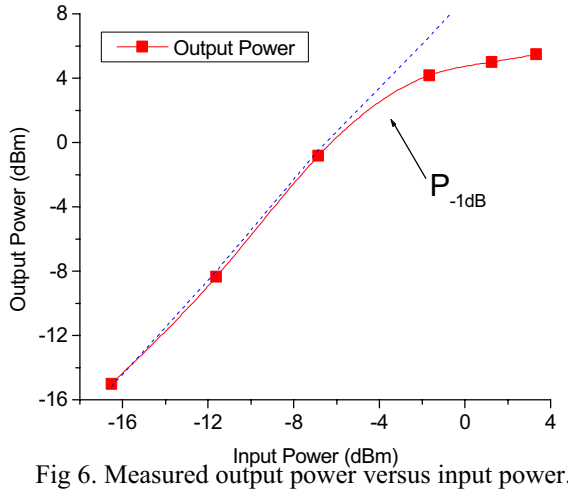

Fig 6. Measured output power versus input power.

The simulated start up transients of the low power amplifier is shown in Fig 7. For a transceiver with 2.5% duty cycle transmitting an average data rate of 10kbits/sec, the bit time is 2.5µs. As shown in Fig. 5, the start up time is 25ns, which constitute only a 1% overhead.

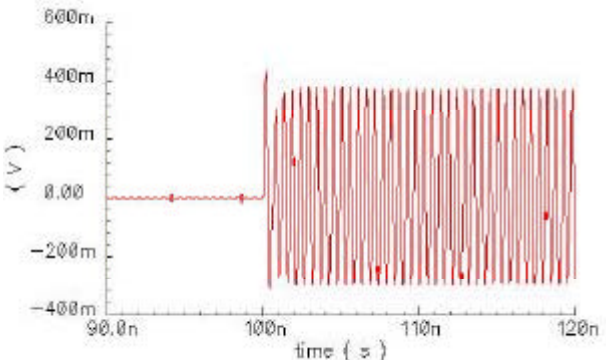

Fig 7. Start up transients of the low power amplifier.

4. CONCLUSION

Ad-hoc wireless sensor networks poised new challenges in low power wireless transceiver design. In a sensor node, energy is most precious resource and the transmitted power is comparable to the circuit power. Thus, though linear power amplifiers have lower drain efficiency, they have lower drive power and are still good candidates for low power amplifier in sensor nodes.

This paper addresses the design and implementation of a class A/B low power amplifier suitable for wireless sensor networks. Several design techniques are used to maximize the efficiency of the amplifier. The amplifier achieved 35% drain efficiency and 26% PAE while delivering 2.6mW at 1.92 GHz with 1.2V supply.

5. ACKNOWLEDGEMENTS

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